Minimizing Single Event Upset Effects Using Synopsys

This application note gives an overview of some single event upset (SEU) resistant design techniques and describes how to implement these techniques using Synopsys. Familiarity with the Synopsys FPGA Compiler tool and "dc_shell" script language is assumed. For additional information about the use of the Synopsys FPGA Compiler tools with Actel devices and general synthesis methodology, refer to the Actel *Synopsys Synthesis Methodology Guide*. For additional information about radiation resistant design techniques, refer to the *Design Techniques for RadHard FPGAs* Application Note. Both are available on the Actel Web site (http://www.actel.com).

Background and Terminology

The Actel ACT 2, ACT 3, 3200DX, and 42MX device families contain two types of logic modules, sequential modules (S-modules) and combinatorial modules (C-modules). S-modules contain a sequential logic element and some combinatorial logic. C-modules contain only combinatorial logic. Flip-flops and latches can be implemented using the sequential logic element of an S-module (S-FF) or by using combinatorial logic (CC-FF). The combinatorial logic in a CC-FF may come from the combinatorial portion of an S-module, from a C-module, or from both.

The 54SX device family also contains two types of logic modules, register cells (R-cells) and combinatorial cells (C-cells). R-cells contain only a sequential logic element. C-cells contain only combinatorial logic. Flip-flops and latches currently can only be implemented using the sequential logic element of an R-cell, also referred to as an S-FF in this Application Note.

The ACT 1 and 40MX device families contain only C-modules. All flip-flops and latches are implemented as CC-FFs.

SEU Resistant Design Techniques

The resistance of a device to SEU effects can be influenced by using certain logic design techniques. The default technique, using S-FFs, produces designs that are the most susceptible to SEU effects. Because ACT 1 and 40MX devices do not have S-modules, S-FFs cannot be implemented in these devices.

In addition to the default there are two SEU resistant design techniques that can be used in Actel devices using Synopsys. In order of increasing resistance to SEU effects the techniques are: using CC-FFs and using triple voting. A single design may use any or all of these design techniques.

Using CC-FFs

Using CC-FFs produces designs that are more resistant to SEU effects than designs using S-FFs. CC-FFs are used by default in ACT 1 and 40MX devices because these devices only contain CC-FFs. CC-FFs cannot currently be implemented in 54SX devices. CC-FFs typically use twice the area resources of S-FFs.

Figure 1 is an example "dc_shell" script that illustrates how to synthesize a design using only CC-FFs. The "sequential_combinatorial" script referenced in the example is available for the ACT 2, ACT 3, 3200DX, and 42MX device families and is located in the "$ACT_SYNOPDIR/lib/synop/scripts/<act_fam>" directory. This script is run after the Actel Synopsys setup script (actsetup.scr) but before synthesis. Table 1 lists the flip-flops and latches that are used to implement CC-FFs in a design.

Using Triple Voting

Using triple voting, also called triple module redundancy (TMR), produces designs that are the most resistant to SEU effects. Instead of a single flip-flop, triple voting uses three flip-flops leading to a majority gate voting circuit. This way, if one flip-flop is accidentally flipped to the wrong state, the other two out-vote it and the correct value is propagated to the rest of the circuit. Because of the cost (typically three to four times the area and two times the delay required for S-FF implementations), triple voting is usually implemented using S-FFs. Actel currently does not provide scripts to implement latches using triple voting. Scripts will be available in a future release.

Figure 2 is an example "dc_shell" script that illustrates how to synthesize a design using triple voting. The "sequential_triple_voting" script referenced in the example is available for the ACT 2, ACT 3, 3200DX, and 42MX device families and is located in the "$ACT_SYNOPDIR/lib/synop/scripts/<act_fam>" directory. A script for the 54SX device family will be available in a future release. This script is run after the Actel Synopsys setup script (actsetup.scr) but before synthesis. Note that there is an extra link step when specifying triple module voting that is not required when specifying CC-FFs.

```
include actsetup.scr /*Actel/Synopsys setup script */
read -f vhdl my_design.vhd /* Read in “my_design” VHDL file */

current_design my_design /* Set the design level */
create_clock -period 20 clk /* Create master clock */
set_dont_touch_network clk /* Avoid adding any buffers to clock network */

set_port_is_pad /* Set for I/O pads */
insert_pads /* Inserting I/Os */

include sequential_combinatorial /* Script to specify CC-FFs and latches */

check_design /* Check design for DRC problems */
compile -map_effort medium /* Synthesize design */

write -f edif -h -o my_design.edn /* Save the EDIF netlist */
write my_design.db /* Save “my_design” in Synopsys DB format */

quit
```

Figure 1 • *Example Synopsys Script to Implement CC-FFs in a Design*

```
include actsetup.scr /* Actel/Synopsys setup script */
read -f vhdl my_design.vhd /* Read in “my_design” VHDL file */

current_design my_design /* Set the design level */
create_clock -period 20 clk /* Create master clock */
set_dont_touch_network clk /* Avoid adding any buffers to clock network */

set_port_is_pad /* Set for IO pads */
insert_pads /* Inserting IOs */

include sequential_triple_voting /* Script to specify triple voting */

check_design /* Check design for DRC problems */
compile -map_effort medium /* Synthesize design */

set_local_library tmrlib.db /* Specify Actel library for link step below */
link    /* Perform link step - required when specifying triple voting */

write -f edif -h -o after_my_design.edn /* Save the EDIF netlist */
write my_design.db /* Save “my_design” in Synopsys DB format */

quit
```

Figure 2 • *Example Synopsys Script to Implement Triple Voting in a Design*

Table 1 • *Flip-Flops and Latches Used for CC-FF Implementations*

DF1_CC	D-Type Flip-Flop
DF1A_CC	D-Type Flip-Flop, Active Low Output
DF1B_CC	D-Type Flip-Flop, Active Low Clock
DF1C_CC	D-Type Flip-Flop, Active Low Clock and Output
DFE_CC	D-Type Flip-Flop, Active High Enable
DFE1B_CC	D-Type Flip-Flop, Active Low Enable
DFE1C_CC	D-Type Flip-Flop, Active Low Enable and Clock
DFEA_CC	D-Type Flip-Flop, Enable and Active low clock
DFM_CC	D-Type Flip-Flop, 2-input Multiplexed Data
DFP1_CC	D-Type Flip-Flop, Active High Preset
DFP1A_CC	D- Type Flip-Flop, Active High Preset & Active low clock
DFP1B_CC	D-Type Flip-Flop, Active Low Preset
DFP1D_CC	D-Type Flip-Flop, Active Low Preset & Active Low Clock
DFPC_CC	D-Type Flip-Flop, Active High preset & Active Low Clear & Active High Clock
DFPCA_CC	D-Type Flip-Flop, Active High Preset & Active Low Clear & Active Low Clock
DFC1A_CC	D-Type Flip-Flop, Active High clear and Active Low clock
DFC1B_CC	D-Type Flip-Flop, Active Low Clear
DFC1D_CC	D-Type Flip-Flop, Active Low Clear and Clock
DFMA_CC	D-Type Flip-Flop, 2-input Multiplexed Data and Active Low Clock
DFM1B_CC	D-Type Flip-Flop, 2-input Multiplexed Data and Active Low Output
DFM1C_CC	D-Type Flip-Flop, 2-input Multiplexed Data and Active Low Clock and Output
DLC1	Data Latch, Active High Clear
DLC1A	Data Latch, Active High Clear & Active Low Clock
DLE2C	Data Latch, Active Low Enable & Active Low Clock & Active High Clear
DLE3B	Data Latch, Active Low Enable & Active High Preset & Active Low Clock
DLE3C	Data Latch, Active Low Enable & Active Low Preset & Active Low Clock
DLP1	Data Latch, Active High Preset & Active High Clock
DLP1A	Data Latch, Active High Preset & Active Low Clock
DLP1B	Data Latch, Active Low Preset & Active High Clock
DLP1C	Data Latch, Active Low Preset & Active Low Clock

Additional Information

For additional information about designing radiation resistant devices, visit the following Web site:

http://www.actel.com/products/radhard.html

If you have any comments or suggestions about Actel's line of radiation resistant devices, e-mail Actel at radhard.designer@actel.com. For technical support contact the Actel Customer Application Center at 1-800-262-1060 or tech@actel.com.

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