

## 40MX and 42MX FPGA Families

---

Actel now offers a '-3' speed grade option for the A42MX09, A42MX16, A42MX24, and A42MX36 devices.

This addendum contains only the '-3' speed grade numbers. For '-2', '-1', 'Std', and '-F' numbers, please refer to the Timing Characteristics Tables on pages 47 through 72 in the standalone *40MX and 42MX FPGA Families* data sheet and on pages 145 through 170 of the *1999 Actel FPGA Data Book*.

## A42MX09 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )

Logic Module Propagation Delays <sup>1</sup>		‘-3’ Speed		
Parameter	Description	Min.	Max.	Units
$t_{PD1}$	Single Module		1.20	ns
$t_{CO}$	Sequential Clock-to-Q		1.29	ns
$t_{GO}$	Latch G-to-Q		1.23	ns
$t_{RS}$	Flip-Flop (Latch) Reset-to-Q		1.24	ns
Predicted Routing Delays <sup>2</sup>				
$t_{RD1}$	FO=1 Routing Delay		0.69	ns
$t_{RD2}$	FO=2 Routing Delay		0.92	ns
$t_{RD3}$	FO=3 Routing Delay		1.15	ns
$t_{RD4}$	FO=4 Routing Delay		1.38	ns
$t_{RD8}$	FO=8 Routing Delay		2.34	ns
Sequential Timing Characteristics <sup>3, 4</sup>				
$t_{SUD}$	Flip-Flop (Latch) Data Input Set-Up	0.32		ns
$t_{HD}$	Flip-Flop (Latch) Data Input Hold	0.00		ns
$t_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.41		ns
$t_{HENA}$	Flip-Flop (Latch) Enable Hold	0.00		ns
$t_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	3.39		ns
$t_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.45		ns
$t_A$	Flip-Flop Clock Input Period	3.45		ns
$t_{INH}$	Input Buffer Latch Hold	0.00		ns
$t_{INSU}$	Input Buffer Latch Set-Up	0.27		ns
$t_{OUTH}$	Output Buffer Latch Hold	0.00		ns
$t_{OUTSU}$	Output Buffer Latch Set-Up	0.27		ns
$f_{MAX}$	Flip-Flop (Latch) Clock Frequency		268.13	MHz

### Notes:

1. For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			‘-3’ Speed		
Parameter	Description		Min.	Max.	Units
t <sub>INYH</sub>	Pad-to-Y HIGH			1.04	ns
t <sub>INYL</sub>	Pad-to-Y LOW			0.82	ns
t <sub>INGH</sub>	G to Y HIGH			1.29	ns
t <sub>INGL</sub>	G to Y LOW			1.29	ns
Input Module Predicted Routing Delays <sup>1</sup>					
t <sub>IRD1</sub>	FO=1 Routing Delay			2.02	ns
t <sub>IRD2</sub>	FO=2 Routing Delay			2.26	ns
t <sub>IRD3</sub>	FO=3 Routing Delay			2.50	ns
t <sub>IRD4</sub>	FO=4 Routing Delay			2.75	ns
t <sub>IRD8</sub>	FO=8 Routing Delay			3.72	ns
Global Clock Network					
t <sub>CKH</sub>	Input LOW to HIGH	FO = 32		2.43	ns
		FO = 256		2.70	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO = 32		3.53	ns
		FO = 256		3.87	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 32	1.22		ns
		FO = 256	1.31		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 32	1.22		ns
		FO = 256	1.31		ns
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.31	ns
		FO = 256		0.31	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO = 32	0.00		ns
		FO = 256	0.00		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	2.34		ns
		FO = 256	2.19		ns
t <sub>P</sub>	Minimum Period	FO = 32	3.35		ns
		FO = 256	3.69		ns
f <sub>MAX</sub>	Maximum Frequency	FO = 32		295.63	MHz
		FO = 256		268.13	MHz

**Note:**

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst case performance

## A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'-3' Speed		
Parameter	Description	Min.	Max.	Units
<b>TTL Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		2.44	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.87	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.64	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.92	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		4.90	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		5.34	ns
t <sub>GLH</sub>	G-to-Pad HIGH		2.61	ns
t <sub>GHL</sub>	G-to-Pad LOW		2.61	ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.49		ns
t <sub>LH</sub>	I/O Latch Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.20	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.36	ns
d <sub>TLH</sub>	Capacity Loading, LOW to HIGH		0.03	ns/pF
d <sub>THL</sub>	Capacity Loading, HIGH to LOW		0.04	ns/pF
<b>CMOS Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		2.44	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.87	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.64	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.92	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		4.90	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		5.34	ns
t <sub>GLH</sub>	G-to-Pad HIGH		4.15	ns
t <sub>GHL</sub>	G-to-Pad LOW		4.15	ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.49		ns
t <sub>LH</sub>	I/O Latch Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.20	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		7.36	ns
d <sub>TLH</sub>	Capacity Loading, LOW to HIGH		0.03	ns/pF
d <sub>THL</sub>	Capacity Loading, HIGH to LOW		0.04	ns/pF

**Notes:**

1. Delays based on 35 pF loading.

## A42MX09 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )

Logic Module Propagation Delays <sup>1</sup>		'-3' Speed		
Parameter	Description	Min.	Max.	Units
t <sub>PD1</sub>	Single Module		1.62	ns
t <sub>CO</sub>	Sequential Clock-to-Q		1.80	ns
t <sub>GO</sub>	Latch G-to-Q		1.69	ns
t <sub>RS</sub>	Flip-Flop (Latch) Reset-to-Q		1.96	ns
Predicted Routing Delays <sup>2</sup>				
t <sub>RD1</sub>	FO=1 Routing Delay		0.99	ns
t <sub>RD2</sub>	FO=2 Routing Delay		1.26	ns
t <sub>RD3</sub>	FO=3 Routing Delay		1.62	ns
t <sub>RD4</sub>	FO=4 Routing Delay		1.89	ns
t <sub>RD8</sub>	FO=8 Routing Delay		3.24	ns
Sequential Timing Characteristics <sup>3, 4</sup>				
t <sub>SUD</sub>	Flip-Flop (Latch) Data Input Set-Up	0.45		ns
t <sub>HD</sub>	Flip-Flop (Latch) Data Input Hold	0.00		ns
t <sub>SUENA</sub>	Flip-Flop (Latch) Enable Set-Up	0.57		ns
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold	0.00		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width	4.74		ns
t <sub>WASYN</sub>	Flip-Flop (Latch) Asynchronous Pulse Width	6.22		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	5.04		ns
t <sub>INH</sub>	Input Buffer Latch Hold	0.00		ns
t <sub>INSU</sub>	Input Buffer Latch Set-Up	0.27		ns
t <sub>OUTH</sub>	Output Buffer Latch Hold	0.00		ns
t <sub>OUTSU</sub>	Output Buffer Latch Set-Up	0.27		ns
f <sub>MAX</sub>	Flip-Flop (Latch) Clock Frequency		160.93	MHz

**Notes:**

1. For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'-3' Speed		
Parameter	Description		Min.	Max.	Units
t <sub>INYH</sub>	Pad-to-Y HIGH			1.47	ns
t <sub>INYL</sub>	Pad-to-Y LOW			1.17	ns
t <sub>INGH</sub>	G to Y HIGH			1.80	ns
t <sub>INGL</sub>	G to Y LOW			1.80	ns
Input Module Predicted Routing Delays <sup>1</sup>					
t <sub>IRD1</sub>	FO=1 Routing Delay			2.84	ns
t <sub>IRD2</sub>	FO=2 Routing Delay			3.15	ns
t <sub>IRD3</sub>	FO=3 Routing Delay			3.51	ns
t <sub>IRD4</sub>	FO=4 Routing Delay			3.87	ns
t <sub>IRD8</sub>	FO=8 Routing Delay			5.22	ns
Global Clock Network					
t <sub>CKH</sub>	Input LOW to HIGH	FO = 32		4.05	ns
		FO = 256		4.50	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO = 32		4.95	ns
		FO = 256		5.40	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 32	1.70		ns
		FO = 256	1.85		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 32	1.70		ns
		FO = 256	1.85		ns
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.42	ns
		FO = 256		0.42	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO = 32	0.00		ns
		FO = 256	0.00		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	3.33		ns
		FO = 256	3.69		ns
t <sub>P</sub>	Minimum Period	FO = 32	5.58		ns
		FO = 256	6.12		ns
f <sub>MAX</sub>	Maximum Frequency	FO = 32		177.43	MHz
		FO = 256		160.93	MHz

**Note:**

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst case performance

## A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'-3' Speed		
Parameter	Description	Min.	Max.	Units
<b>TTL Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		3.41	ns
t <sub>DHL</sub>	Data-to-Pad LOW		4.01	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		3.69	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		4.09	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		6.85	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		7.47	ns
t <sub>GLH</sub>	G-to-Pad HIGH		5.81	ns
t <sub>GHL</sub>	G-to-Pad LOW		5.81	ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.68		ns
t <sub>LH</sub>	I/O Latch Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.73	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.15	ns
d <sub>TLH</sub>	Capacity Loading, LOW to HIGH		0.00	ns/pF
d <sub>THL</sub>	Capacity Loading, HIGH to LOW		0.09	ns/pF
<b>CMOS Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		3.42	ns
t <sub>DHL</sub>	Data-to-Pad LOW		4.05	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		3.69	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		4.09	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		6.85	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		7.47	ns
t <sub>GLH</sub>	G-to-Pad HIGH		5.81	ns
t <sub>GHL</sub>	G-to-Pad LOW		5.81	ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.68		ns
t <sub>LH</sub>	I/O Latch Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.73	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.15	ns
d <sub>TLH</sub>	Capacity Loading, LOW to HIGH		0.04	ns/pF
d <sub>THL</sub>	Capacity Loading, HIGH to LOW		0.05	ns/pF

**Notes:**

1. Delays based on 35 pF loading.

## A42MX16 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )

Logic Module Propagation Delays <sup>1</sup>		'-3' Speed		
Parameter	Description	Min.	Max.	Units
$t_{PD1}$	Single Module		1.37	ns
$t_{CO}$	Sequential Clock-to-Q		1.44	ns
$t_{GO}$	Latch G-to-Q		1.37	ns
$t_{RS}$	Flip-Flop (Latch) Reset-to-Q		1.57	ns
Predicted Routing Delays <sup>2</sup>				
$t_{RD1}$	FO=1 Routing Delay		0.77	ns
$t_{RD2}$	FO=2 Routing Delay		1.04	ns
$t_{RD3}$	FO=3 Routing Delay		1.29	ns
$t_{RD4}$	FO=4 Routing Delay		1.55	ns
$t_{RD8}$	FO=8 Routing Delay		2.57	ns
Sequential Timing Characteristics <sup>3,4</sup>				
$t_{SUD}$	Flip-Flop (Latch) Data Input Set-Up	0.32		ns
$t_{HD}$	Flip-Flop (Latch) Data Input Hold	0.00		ns
$t_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.68		ns
$t_{HENA}$	Flip-Flop (Latch) Enable Hold	0.00		ns
$t_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	3.40		ns
$t_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.46		ns
$t_A$	Flip-Flop Clock Input Period	6.80		ns
$t_{INH}$	Input Buffer Latch Hold	0.00		ns
$t_{INSU}$	Input Buffer Latch Set-Up	0.49		ns
$t_{OUTH}$	Output Buffer Latch Hold	0.00		ns
$t_{OUTSU}$	Output Buffer Latch Set-Up	0.49		ns
$f_{MAX}$	Flip-Flop (Latch) Clock Frequency		214.50	MHz

### Notes:

1. For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.



## A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			‘-3’ Speed		
Parameter	Description		Min.	Max.	Units
t <sub>INYH</sub>	Pad-to-Y HIGH			1.05	ns
t <sub>INYL</sub>	Pad-to-Y LOW			0.81	ns
t <sub>INGH</sub>	G to Y HIGH			1.40	ns
t <sub>INGL</sub>	G to Y LOW			1.40	ns
Input Module Predicted Routing Delays <sup>1</sup>					
t <sub>IRD1</sub>	FO=1 Routing Delay			1.83	ns
t <sub>IRD2</sub>	FO=2 Routing Delay			2.09	ns
t <sub>IRD3</sub>	FO=3 Routing Delay			2.34	ns
t <sub>IRD4</sub>	FO=4 Routing Delay			2.60	ns
t <sub>IRD8</sub>	FO=8 Routing Delay			3.63	ns
Global Clock Network					
t <sub>CKH</sub>	Input LOW to HIGH	FO = 32		2.61	ns
		FO = 384		2.88	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO = 32		3.78	ns
		FO = 384		4.46	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 32	3.18		ns
		FO = 384	3.65		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 32	3.18		ns
		FO = 384	3.65		ns
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.34	ns
		FO = 384		0.34	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO = 32	0.00		ns
		FO = 384	0.00		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	2.77		ns
		FO = 384	3.18		ns
t <sub>P</sub>	Minimum Period	FO = 32	4.19		ns
		FO = 384	4.61		ns
f <sub>MAX</sub>	Maximum Frequency	FO = 32		236.50	MHz
		FO = 384		214.50	MHz

**Note:**

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'-3' Speed		
Parameter	Description	Min.	Max.	Units
<b>TTL Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		2.51	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.94	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.70	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.99	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		5.42	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		5.01	ns
t <sub>GLH</sub>	G-to-Pad HIGH		2.88	ns
t <sub>GHL</sub>	G-to-Pad LOW		2.88	ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.65	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.04	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.03	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.04	ns/pF
<b>CMOS Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		3.20	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.46	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.70	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.99	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		5.42	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		5.01	ns
t <sub>GLH</sub>	G-to-Pad HIGH		5.07	ns
t <sub>GHL</sub>	G-to-Pad LOW		5.07	ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		5.65	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.04	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.03	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.04	ns/pF

**Notes:**

1. Delays based on 35 pF loading.

## A42MX16 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )

Logic Module Propagation Delays <sup>1</sup>		‘-3’ Speed		
Parameter	Description	Min.	Max.	Units
t <sub>PD1</sub>	Single Module		1.92	ns
t <sub>CO</sub>	Sequential Clock-to-Q		2.02	ns
t <sub>GO</sub>	Latch G-to-Q		1.92	ns
t <sub>RS</sub>	Flip-Flop (Latch) Reset-to-Q		2.20	ns
Predicted Routing Delays <sup>2</sup>				
t <sub>RD1</sub>	FO=1 Routing Delay		1.09	ns
t <sub>RD2</sub>	FO=2 Routing Delay		1.45	ns
t <sub>RD3</sub>	FO=3 Routing Delay		1.81	ns
t <sub>RD4</sub>	FO=4 Routing Delay		2.16	ns
t <sub>RD8</sub>	FO=8 Routing Delay		3.60	ns
Sequential Timing Characteristics <sup>3, 4</sup>				
t <sub>SUD</sub>	Flip-Flop (Latch) Data Input Set-Up	0.45		ns
t <sub>HD</sub>	Flip-Flop (Latch) Data Input Hold	0.00		ns
t <sub>SUENA</sub>	Flip-Flop (Latch) Enable Set-Up	0.95		ns
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold	0.00		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width	4.76		ns
t <sub>WASYN</sub>	Flip-Flop (Latch) Asynchronous Pulse Width	6.24		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	9.52		ns
t <sub>INH</sub>	Input Buffer Latch Hold	0.00		ns
t <sub>INSU</sub>	Input Buffer Latch Set-Up	0.68		ns
t <sub>OUTH</sub>	Output Buffer Latch Hold	0.00		ns
t <sub>OUTSU</sub>	Output Buffer Latch Set-Up	0.68		ns
f <sub>MAX</sub>	Flip-Flop (Latch) Clock Frequency		128.70	MHz

**Notes:**

1. For dual-module macros use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'-3' Speed		
Parameter	Description		Min.	Max.	Units
t <sub>INYH</sub>	Pad-to-Y HIGH			1.48	ns
t <sub>INYL</sub>	Pad-to-Y LOW			1.13	ns
t <sub>INGH</sub>	G to Y HIGH			1.96	ns
t <sub>INGL</sub>	G to Y LOW			1.96	ns
Input Module Predicted Routing Delays <sup>1</sup>					
t <sub>IRD1</sub>	FO=1 Routing Delay			2.57	ns
t <sub>IRD2</sub>	FO=2 Routing Delay			2.92	ns
t <sub>IRD3</sub>	FO=3 Routing Delay			3.28	ns
t <sub>IRD4</sub>	FO=4 Routing Delay			3.64	ns
t <sub>IRD8</sub>	FO=8 Routing Delay			5.08	ns
Global Clock Network					
t <sub>CKH</sub>	Input LOW to HIGH	FO = 32		4.35	ns
		FO = 384		4.80	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO = 32		5.29	ns
		FO = 384		6.24	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 32	5.67		ns
		FO = 384	6.62		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 32	5.29		ns
		FO = 384	6.24		ns
t <sub>CKSW</sub>	Maximum Skew	FO = 32		0.48	ns
		FO = 384		2.18	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO = 32	0.00		ns
		FO = 384	0.00		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO = 32	3.88		ns
		FO = 384	4.45		ns
t <sub>P</sub>	Minimum Period	FO = 32	6.98		ns
		FO = 384	7.70		ns
f <sub>MAX</sub>	Maximum Frequency	FO = 32		141.90	MHz
		FO = 384		128.70	MHz

**Note:**

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		‘-3’ Speed		
Parameter	Description	Min.	Max.	Units
<b>TTL Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		3.52	ns
t <sub>DHL</sub>	Data-to-Pad LOW		4.12	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		3.78	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		4.18	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		7.58	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		7.01	ns
t <sub>GLH</sub>	G-to-Pad HIGH		4.77	ns
t <sub>GHL</sub>	G-to-Pad LOW		4.77	ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.04	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.25	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.04	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.05	ns/pF
<b>CMOS Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		4.48	ns
t <sub>DHL</sub>	Data-to-Pad LOW		3.44	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		3.78	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		4.18	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		7.58	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		7.01	ns
t <sub>GLH</sub>	G-to-Pad HIGH		7.10	ns
t <sub>GHL</sub>	G-to-Pad LOW		7.10	ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.04	ns
t <sub>ACO</sub>	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.25	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.04	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.05	ns/pF

**Notes:**

1. Delays based on 35 pF loading.

## A42MX24 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )

		Preliminary Information		
Logic Module Propagation Delays <sup>1</sup>		‘-3 Speed		
Parameter	Description	Min.	Max.	Units
<b>Combinatorial Functions</b>				
$t_{PD}$	Internal Array Module Delay		1.18	ns
$t_{PDD}$	Internal Decode Module Delay		1.43	ns
<b>Predicted Routing Delays<sup>2</sup></b>				
$t_{RD1}$	FO=1 Routing Delay		0.80	ns
$t_{RD2}$	FO=2 Routing Delay		1.04	ns
$t_{RD3}$	FO=3 Routing Delay		1.26	ns
$t_{RD4}$	FO=4 Routing Delay		1.49	ns
$t_{RD5}$	FO=8 Routing Delay		2.40	ns
<b>Sequential Timing Characteristics<sup>3, 4</sup></b>				
$t_{CO}$	Flip-Flop Clock-to-Output		1.29	ns
$t_{GO}$	Latch Gate-to-Output		1.18	ns
$t_{SU}$	Flip-Flop (Latch) Set-Up Time	0.32		ns
$t_H$	Flip-Flop (Latch) Hold Time	0.00		ns
$t_{RO}$	Flip-Flop (Latch) Reset-to-Output		1.40	ns
$t_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.41		ns
$t_{HENA}$	Flip-Flop (Latch) Enable Hold	0.00		ns
$t_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	3.31		ns
$t_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.35		ns

### Notes:

- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
- Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information		
Input Module Propagation Delays			'-3' Speed		
Parameter	Description		Min.	Max.	Units
t <sub>INPY</sub>	Input Data Pad-to-Y			1.03	ns
t <sub>INGO</sub>	Input Latch Gate-to-Output			1.25	ns
t <sub>INH</sub>	Input Latch Hold		0.00		ns
t <sub>INSU</sub>	Input Latch Set-Up		0.48		ns
t <sub>ILA</sub>	Latch Active Pulse Width		4.66		ns
Input Module Predicted Routing Delays <sup>1</sup>					
t <sub>IRD1</sub>	FO=1 Routing Delay			1.83	ns
t <sub>IRD2</sub>	FO=2 Routing Delay			2.06	ns
t <sub>IRD3</sub>	FO=3 Routing Delay			2.29	ns
t <sub>IRD4</sub>	FO=4 Routing Delay			2.52	ns
t <sub>IRD8</sub>	FO=8 Routing Delay			3.43	ns
Global Clock Network					
t <sub>CKH</sub>	Input LOW to HIGH	FO=32		2.61	ns
		FO=486		2.88	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO=32		3.65	ns
		FO=486		4.26	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO=32	2.16		ns
		FO=486	2.37		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO=32	2.16		ns
		FO=486	2.37		ns
t <sub>CKSW</sub>	Maximum Skew	FO=32		0.54	ns
		FO=486		0.54	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO=32	0.00		ns
		FO=486	0.00		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO=32	2.77		ns
		FO=486	3.31		ns
t <sub>P</sub>	Minimum Period (1/f <sub>MAX</sub> )	FO=32	4.71		ns
		FO=486	5.14		ns
f <sub>MAX</sub>	Maximum Datapath Frequency	FO=32		210.38	MHz
		FO=486		192.50	MHz

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

## A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Output Module Timing		-3 Speed		
Parameter	Description	Min.	Max.	Units
<b>TTL Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		2.43	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.84	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.54	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.82	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		5.15	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		4.80	ns
t <sub>GLH</sub>	G-to-Pad HIGH		2.88	ns
t <sub>GHL</sub>	G-to-Pad LOW		2.88	ns
t <sub>LSU</sub>	I/O Latch Output Set-Up	0.48		ns
t <sub>LH</sub>	I/O Latch Output Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.47	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.60	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.04	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.03	ns/pF
<b>CMOS Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		3.11	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.35	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.54	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.82	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		5.15	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		4.80	ns
t <sub>GLH</sub>	G-to-Pad HIGH		4.88	ns
t <sub>GHL</sub>	G-to-Pad LOW		4.88	ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.48		ns
t <sub>LH</sub>	I/O Latch Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.47	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.60	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.04	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.03	ns/pF

**Notes:**

1. Delays based on 35 pF loading.



## A42MX24 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )

		Preliminary Information		
Logic Module Propagation Delays <sup>1</sup>		‘-3 Speed		
Parameter	Description	Min.	Max.	Units
<b>Combinatorial Functions</b>				
$t_{PD}$	Internal Array Module Delay		2.01	ns
$t_{PDD}$	Internal Decode Module Delay		1.13	ns
<b>Predicted Routing Delays<sup>2</sup></b>				
$t_{RD1}$	FO=1 Routing Delay		1.66	ns
$t_{RD2}$	FO=2 Routing Delay		2.01	ns
$t_{RD3}$	FO=3 Routing Delay		1.13	ns
$t_{RD4}$	FO=4 Routing Delay		1.45	ns
$t_{RD5}$	FO=8 Routing Delay		1.76	ns
<b>Sequential Timing Characteristics<sup>3, 4</sup></b>				
$t_{CO}$	Flip-Flop Clock-to-Output		2.09	ns
$t_{GO}$	Latch Gate-to-Output		3.37	ns
$t_{SU}$	Flip-Flop (Latch) Set-Up Time	0.44		ns
$t_H$	Flip-Flop (Latch) Hold Time	0.00		ns
$t_{RO}$	Flip-Flop (Latch) Reset-to-Output		1.95	ns
$t_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.57		ns
$t_{HENA}$	Flip-Flop (Latch) Enable Hold	0.00		ns
$t_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	4.64		ns
$t_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	6.08		ns

**Notes:**

1. For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information		
Input Module Propagation Delays			'-3' Speed		
Parameter	Description		Min.	Max.	Units
t <sub>INPY</sub>	Input Data Pad-to-Y			1.44	ns
t <sub>INGO</sub>	Input Latch Gate-to-Output			1.75	ns
t <sub>INH</sub>	Input Latch Hold		0.00		ns
t <sub>INSU</sub>	Input Latch Set-Up		0.67		ns
t <sub>ILA</sub>	Latch Active Pulse Width		6.53		ns
Input Module Predicted Routing Delays <sup>1</sup>					
t <sub>IRD1</sub>	FO=1 Routing Delay			2.57	ns
t <sub>IRD2</sub>	FO=2 Routing Delay			2.88	ns
t <sub>IRD3</sub>	FO=3 Routing Delay			3.20	ns
t <sub>IRD4</sub>	FO=4 Routing Delay			3.53	ns
t <sub>IRD8</sub>	FO=8 Routing Delay			4.80	ns
Global Clock Network					
t <sub>CKH</sub>	Input LOW to HIGH	FO=32		4.35	ns
		FO=486		4.80	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO=32		5.10	ns
		FO=486		5.96	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO=32	3.02		ns
		FO=486	3.31		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO=32	3.02		ns
		FO=486	3.31		ns
t <sub>CKSW</sub>	Maximum Skew	FO=32		0.76	ns
		FO=486		0.76	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO=32	0.00		ns
		FO=486	0.00		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO=32	3.88		ns
		FO=486	4.64		ns
t <sub>P</sub>	Minimum Period (1/f <sub>MAX</sub> )	FO=32	7.84		ns
		FO=486	8.57		ns
f <sub>MAX</sub>	Maximum Datapath Frequency	FO=32		126.23	MHz
		FO=486		115.50	MHz

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

## A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Output Module Timing		‘–3 Speed		
Parameter	Description	Min.	Max.	Units
<b>TTL Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		3.40	ns
t <sub>DHL</sub>	Data-to-Pad LOW		3.97	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		3.56	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		3.94	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		7.20	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		6.71	ns
t <sub>GLH</sub>	G-to-Pad HIGH		4.77	ns
t <sub>GHL</sub>	G-to-Pad LOW		4.77	ns
t <sub>LSU</sub>	I/O Latch Output Set-Up	0.67		ns
t <sub>LH</sub>	I/O Latch Output Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.66	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		14.84	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.05	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.04	ns/pF
<b>CMOS Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		4.79	ns
t <sub>DHL</sub>	Data-to-Pad LOW		3.51	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		3.56	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		3.38	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		7.20	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		6.71	ns
t <sub>GLH</sub>	G-to-Pad HIGH		6.83	ns
t <sub>GHL</sub>	G-to-Pad LOW		6.83	ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.67		ns
t <sub>LH</sub>	I/O Latch Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.66	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		14.84	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.05	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.04	ns/pF

**Notes:**

1. Delays based on 35 pF loading.

## A42MX36 Timing Characteristics (Nominal 5.0V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )

		Preliminary Information		
Logic Module Propagation Delays		'-3 Speed		
Parameter	Description	Min.	Max.	Units
<b>Combinatorial Functions</b>				
$t_{PD}$	Internal Array Module Delay		1.31	ns
$t_{PDD}$	Internal Decode Module Delay		1.60	ns
<b>Predicted Module Routing Delays</b>				
$t_{RD1}$	FO=1 Routing Delay		0.94	ns
$t_{RD2}$	FO=2 Routing Delay		1.28	ns
$t_{RD3}$	FO=3 Routing Delay		1.61	ns
$t_{RD4}$	FO=4 Routing Delay		1.96	ns
$t_{RD5}$	FO=8 Routing Delay		3.31	ns
$t_{RDD}$	Decode-to-Output Routing Delay		0.34	ns
<b>Sequential Timing Characteristics</b>				
$t_{CO}$	Flip-Flop Clock-to-Output		1.29	ns
$t_{GO}$	Latch Gate-to-Output		1.29	ns
$t_{SU}$	Flip-Flop (Latch) Set-Up Time	0.32		ns
$t_H$	Flip-Flop (Latch) Hold Time	0.00		ns
$t_{RO}$	Flip-Flop (Latch) Reset-to-Output		1.56	ns
$t_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.68		ns
$t_{HENA}$	Flip-Flop (Latch) Enable Hold	0.00		ns
$t_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	3.31		ns
$t_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.35		ns

## A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Logic Module Timing		‘-3’ Speed		
Parameter	Description	Min.	Max.	Units
<b>Synchronous SRAM Operations</b>				
t <sub>RC</sub>	Read Cycle Time	6.75		ns
t <sub>WC</sub>	Write Cycle Time	6.75		ns
t <sub>RCKHL</sub>	Clock HIGH/LOW Time	3.38		ns
t <sub>RCO</sub>	Data Valid After Clock HIGH/LOW		3.38	ns
t <sub>ADSU</sub>	Address/Data Set-Up Time	1.62		ns
t <sub>ADH</sub>	Address/Data Hold Time	0.00		ns
t <sub>RENSU</sub>	Read Enable Set-Up	0.61		ns
t <sub>RENH</sub>	Read Enable Hold	3.38		ns
t <sub>WENSU</sub>	Write Enable Set-Up	2.70		ns
t <sub>WENH</sub>	Write Enable Hold	0.00		ns
t <sub>BENS</sub>	Block Enable Set-Up	2.77		ns
t <sub>BENH</sub>	Block Enable Hold	0.00		ns
<b>Asynchronous SRAM Operations</b>				
t <sub>RPD</sub>	Asynchronous Access Time		8.10	ns
t <sub>RDADV</sub>	Read Address Valid	8.78		ns
t <sub>ADSU</sub>	Address/Data Set-Up Time	1.62		ns
t <sub>ADH</sub>	Address/Data Hold Time	0.00		ns
t <sub>RENSUA</sub>	Read Enable Set-Up to Address Valid	0.61		ns
t <sub>RENHA</sub>	Read Enable Hold	3.38		ns
t <sub>WENSU</sub>	Write Enable Set-Up	2.70		ns
t <sub>WENH</sub>	Write Enable Hold	0.00		ns
t <sub>DOH</sub>	Data Out Hold Time		1.22	ns

## A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

			Advanced Information		
Input Module Propagation Delays			'-3' Speed		
Parameter	Description		Min.	Max.	Units
t <sub>INPY</sub>	Input Data Pad-to-Y			1.03	ns
t <sub>INGO</sub>	Input Latch Gate-to-Output <sup>1</sup>			1.40	ns
t <sub>INH</sub>	Input Latch Hold <sup>1</sup>		0.00		ns
t <sub>INSU</sub>	Input Latch Set-Up <sup>1</sup>		0.48		ns
t <sub>ILA</sub>	Latch Active Pulse Width <sup>1</sup>		4.66		ns
Input Module Predicted Routing Delays					
t <sub>IRD1</sub>	FO=1 Routing Delay			1.96	ns
t <sub>IRD2</sub>	FO=2 Routing Delay			2.30	ns
t <sub>IRD3</sub>	FO=3 Routing Delay			2.64	ns
t <sub>IRD4</sub>	FO=4 Routing Delay			2.99	ns
t <sub>IRD8</sub>	FO=8 Routing Delay			4.34	ns
Global Clock Network					
t <sub>CKH</sub>	Input LOW to HIGH	FO=32		2.73	ns
		FO=635		3.00	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO=32		3.78	ns
		FO=635		4.86	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO=32	1.76		ns
		FO=635	1.96		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO=32	1.76		ns
		FO=635	1.96		ns
t <sub>CKSW</sub>	Maximum Skew	FO=32		0.75	ns
		FO=635		0.75	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO=32	0.00		ns
		FO=635	0.00		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO=32	2.84		ns
		FO=635	3.31		ns
t <sub>P</sub>	Minimum Period (1/f <sub>MAX</sub> )	FO=32	5.49		ns
		FO=635	5.95		ns
f <sub>HMAX</sub>	Maximum Datapath Frequency	FO=32		180.13	MHz
		FO=635		166.38	MHz

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

## A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)

(Worst-Case Commercial Conditions)

		Advanced Information		
Output Module Timing		‘-3’ Speed		
Parameter	Description	Min.	Max.	Units
<b>TTL Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		2.56	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.96	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.66	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.93	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		5.26	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		4.91	ns
t <sub>GLH</sub>	G-to-Pad HIGH		2.94	ns
t <sub>GHL</sub>	G-to-Pad LOW		2.94	ns
t <sub>LSU</sub>	I/O Latch Output Set-Up	0.48		ns
t <sub>LH</sub>	I/O Latch Output Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.67	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.77	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.07	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.07	ns/pF
<b>CMOS Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		3.53	ns
t <sub>DHL</sub>	Data-to-Pad LOW		2.46	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		2.66	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		2.93	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		5.26	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		4.91	ns
t <sub>GLH</sub>	G-to-Pad HIGH		5.03	ns
t <sub>GHL</sub>	G-to-Pad LOW		5.03	ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.48		ns
t <sub>LH</sub>	I/O Latch Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.67	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.77	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.07	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.07	ns/pF

**Notes:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

## A42MX36 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )

		Preliminary Information		
Logic Module Propagation Delays		'-3' Speed		
Parameter	Description	Min.	Max.	Units
<b>Combinatorial Functions</b>				
$t_{PD}$	Internal Array Module Delay		1.85	ns
$t_{PDD}$	Internal Decode Module Delay		2.24	ns
<b>Predicted Module Routing Delays</b>				
$t_{RD1}$	FO=1 Routing Delay		1.31	ns
$t_{RD2}$	FO=2 Routing Delay		1.78	ns
$t_{RD3}$	FO=3 Routing Delay		2.26	ns
$t_{RD4}$	FO=4 Routing Delay		2.75	ns
$t_{RD5}$	FO=8 Routing Delay		4.64	ns
$t_{RDD}$	Decode-to-Output Routing Delay		0.48	ns
<b>Sequential Timing Characteristics</b>				
$t_{CO}$	Flip-Flop Clock-to-Output		1.80	ns
$t_{GO}$	Latch Gate-to-Output		1.80	ns
$t_{SU}$	Flip-Flop (Latch) Set-Up Time	0.44		ns
$t_H$	Flip-Flop (Latch) Hold Time	0.00		ns
$t_{RO}$	Flip-Flop (Latch) Reset-to-Output		2.19	ns
$t_{SUENA}$	Flip-Flop (Latch) Enable Set-Up	0.99		ns
$t_{HENA}$	Flip-Flop (Latch) Enable Hold	0.00		ns
$t_{WCLKA}$	Flip-Flop (Latch) Clock Active Pulse Width	4.64		ns
$t_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	6.08		ns



## A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Logic Module Timing		‘-3’ Speed		
Parameter	Description	Min.	Max.	Units
<b>Synchronous SRAM Operations</b>				
t <sub>RC</sub>	Read Cycle Time	9.45		ns
t <sub>WC</sub>	Write Cycle Time	9.45		ns
t <sub>RCKHL</sub>	Clock HIGH/LOW Time	4.77		ns
t <sub>RCO</sub>	Data Valid After Clock HIGH/LOW		4.77	ns
t <sub>ADSU</sub>	Address/Data Set-Up Time	2.25		ns
t <sub>ADH</sub>	Address/Data Hold Time	0.00		ns
t <sub>RENSU</sub>	Read Enable Set-Up	0.90		ns
t <sub>RENH</sub>	Read Enable Hold	4.77		ns
t <sub>WENSU</sub>	Write Enable Set-Up	3.78		ns
t <sub>WENH</sub>	Write Enable Hold	0.00		ns
t <sub>BENS</sub>	Block Enable Set-Up	3.87		ns
t <sub>BENH</sub>	Block Enable Hold	0.00		ns
<b>Asynchronous SRAM Operations</b>				
t <sub>RPD</sub>	Asynchronous Access Time		11.34	ns
t <sub>RDADV</sub>	Read Address Valid	12.33		ns
t <sub>ADSU</sub>	Address/Data Set-Up Time	2.25		ns
t <sub>ADH</sub>	Address/Data Hold Time	0.00		ns
t <sub>RENSUA</sub>	Read Enable Set-Up to Address Valid	0.90		ns
t <sub>RENHA</sub>	Read Enable Hold	4.77		ns
t <sub>WENSU</sub>	Write Enable Set-Up	3.78		ns
t <sub>WENH</sub>	Write Enable Hold	0.00		ns
t <sub>DOH</sub>	Data Out Hold Time		1.80	ns

## A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

			Preliminary Information		
Input Module Propagation Delays			'-3' Speed		
Parameter	Description		Min.	Max.	Units
t <sub>INPY</sub>	Input Data Pad-to-Y			1.44	ns
t <sub>INGO</sub>	Input Latch Gate-to-Output <sup>1</sup>			1.95	ns
t <sub>INH</sub>	Input Latch Hold <sup>1</sup>		0.00		ns
t <sub>INSU</sub>	Input Latch Set-Up <sup>1</sup>		0.67		ns
t <sub>ILA</sub>	Latch Active Pulse Width <sup>1</sup>		6.53		ns
Input Module Predicted Routing Delays					
t <sub>IRD1</sub>	FO=1 Routing Delay			2.75	ns
t <sub>IRD2</sub>	FO=2 Routing Delay			3.22	ns
t <sub>IRD3</sub>	FO=3 Routing Delay			3.70	ns
t <sub>IRD4</sub>	FO=4 Routing Delay			4.18	ns
t <sub>IRD8</sub>	FO=8 Routing Delay			6.08	ns
Global Clock Network					
t <sub>CKH</sub>	Input LOW to HIGH	FO=32		4.55	ns
		FO=635		5.00	ns
t <sub>CKL</sub>	Input HIGH to LOW	FO=32		5.29	ns
		FO=635		6.80	ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO=32	2.46		ns
		FO=635	2.75		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO=32	2.46		ns
		FO=635	2.75		ns
t <sub>CKSW</sub>	Maximum Skew	FO=32		1.04	ns
		FO=635		1.04	ns
t <sub>SUEXT</sub>	Input Latch External Set-Up	FO=32	0.00		ns
		FO=635	0.00		ns
t <sub>HEXT</sub>	Input Latch External Hold	FO=32	3.97		ns
		FO=635	4.64		ns
t <sub>P</sub>	Minimum Period (1/f <sub>MAX</sub> )	FO=32	9.16		ns
		FO=635	9.92		ns
f <sub>HMAX</sub>	Maximum Datapath Frequency	FO=32		108.08	MHz
		FO=635		99.83	MHz

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

## A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		
Output Module Timing		‘-3’ Speed		
Parameter	Description	Min.	Max.	Units
<b>TTL Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		3.57	ns
t <sub>DHL</sub>	Data-to-Pad LOW		4.15	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		3.72	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		4.10	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		7.36	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		6.87	ns
t <sub>GLH</sub>	G-to-Pad HIGH		4.91	ns
t <sub>GHL</sub>	G-to-Pad LOW		4.91	ns
t <sub>LSU</sub>	I/O Latch Output Set-Up	0.67		ns
t <sub>LH</sub>	I/O Latch Output Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.94	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.87	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.10	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.10	ns/pF
<b>CMOS Output Module Timing<sup>1</sup></b>				
t <sub>DLH</sub>	Data-to-Pad HIGH		4.94	ns
t <sub>DHL</sub>	Data-to-Pad LOW		3.44	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		3.72	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		4.10	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		7.36	ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		6.87	ns
t <sub>GLH</sub>	G-to-Pad HIGH		7.04	ns
t <sub>GHL</sub>	G-to-Pad LOW		7.04	ns
t <sub>LSU</sub>	I/O Latch Set-Up	0.67		ns
t <sub>LH</sub>	I/O Latch Hold	0.00		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.94	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.87	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.10	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.10	ns/pF

**Notes:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

Actel and the Actel logo are registered trademarks of Actel Corporation.  
All other trademarks are the property of their owners.



<http://www.actel.com>

**Actel Europe Ltd.**

Daneshill House, Lutyens Close  
Basingstoke, Hampshire RG24 8AG  
United Kingdom

**Tel:** +44.(0)1256.305600

**Fax:** +44.(0)1256.355420

**Actel Corporation**

955 East Arques Avenue  
Sunnyvale, California 94086  
USA

**Tel:** 408.739.1010

**Fax:** 408.739.1540

**Actel Asia-Pacific**

EXOS Ebisu Bldg. 4F  
1-24-14 Ebisu Shibuya-ku  
Tokyo 150 Japan

**Tel:** +81.(0)3.3445.7671

**Fax:** +81.(0)3.3445.7668