Verilog®

Simulation Guide

Actel

Windows® and UNIX® Environments

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Table of Contents

Introduction

The *Verilog Simulation Guide* contains information about interfacing the Designer Series FPGA development software with Verilog simulation tools. Refer to the *Designing with Actel* manual for additional information about using the Designer software and the documentation included with your Verilog simulation tool for information about performing simulation.

Document Organization

The *Verilog Simulation Guide* is divided into the following chapters:

Chapter 1 - Setup contains information and procedures about setting up Verilog libraries for use in simulating Actel designs.

Chapter 2 - Design Flow illustrates and describes the design flow for simulating Actel designs using Verilog Simulation tools.

Chapter 3 - Generating Netlists contains information and procedures for generating EDIF and structural Verilog netlists.

Chapter 4 - Simulation contains information and procedures about performing simulation on Actel designs with Verilog simulators.

Appendix A - Product Support provides information about contacting Actel for customer and technical support.

Document Assumptions

The information in this manual is based on the following assumptions:

1. If you are using a PC, you have installed the Designer Series software in the "c:\actel" directory.
2. You have installed a Verilog simulator.
3. You are familiar with UNIX workstations and operating systems.
4. You are familiar with PCs and Windows operating environments.
5. You are familiar with FPGA architecture and FPGA design software.

Document Conventions

The following conventions are used throughout this manual.

Information that is meant to be input by the user is formatted as follows:

```
keyboard input
```

The contents of a file is formatted as follows:

```
file contents
```

Messages that are displayed on the screen appear as follows:

```
Screen Message
```

The <act_fam> variable represents an Actel device family. To reference an actual family, substitute the name of the Actel device when you see this variable. Available families are act1, act2, 1200xl, act3, 3200dx, 40mx, 42mx, and 54sx.

Actel Manuals

The Designer Series software includes printed and on-line manuals. The on-line manuals are in PDF format on the CD-ROM in the "/manuals" directory. These manuals are also installed onto your system when you install the Designer software. To view the on-line manuals, you must install Adobe® Acrobat Reader® from the CD-Rom.

The Designer Series includes the following manuals, which provide additional information on designing Actel FPGAs:

Designing with Actel. This manual describes the design flow and user interface for the Actel Designer Series software, including information about using the ACTgen Macro Builder and ACTmap VHDL Synthesis software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

ACTmap VHDL Synthesis Methodology Guide. This guide contains information, optimization techniques, and procedures to assist designers in the design of Actel devices using ACTmap VHDL.

Silicon Expert User's Guide. This guide contains information and procedures to assist designers in the use of Actel's Silicon Expert tool.

DeskTOP Interface Guide. This guide contains information about using the integrated VeriBest® and Synplicity® CAE software tools with the Actel Designer Series FPGA development tools to create designs for Actel Devices.

Cadence® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

MOTIVE™ Static Timing Analysis Interface Guide. This guide contains information and procedures to assist designers in the use of the MOTIVE software to perform static timing analysis on Actel designs.

Synopsys® Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information and procedures to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Viewlogic Powerview® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Powerview CAE software and the Designer Series software.

Viewlogic Workview Office Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Workview Office CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Silicon Explorer Quick Start. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Designer Series Development System Conversion Guide UNIX® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for UNIX to be compatible with later versions of Designer Series.

Designer Series Development System Conversion Guide Windows Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for Windows to be compatible with later versions of Designer Series.

Actel FPGA Data Book. This guide contains detailed specifications on Actel device families. Information such as propagation delays, device package pinout, derating factors, and power calculations are found in this guide.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

A Guide to ACTgen Macros. This Guide provides descriptions of macros that can be generated using the Actel ACTgen Macro Builder software.

On-Line Help

The Designer Series software comes with on-line help. On-line help specific to each software tool is available in Designer, ACTgen, ACTmap, Silicon Expert, Silicon Explorer, Silicon Sculptor, and APSW.

1 Setup

This chapter contains information about setting up Verilog libraries for use in simulating Actel designs and the directory structure of the libraries. Refer to the documentation included with your Verilog simulator for information about setting up your simulation tool.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R1-1999 or later and IEEE-1364 compliant Verilog simulators. Additionally, this guides contains information about using the PC and UNIX MTI V-System and ModelSim simulators, the UNIX Mentor Graphics QuickHDL simulator, the UNIX Cadence Verilog-XL simulator, the PC and UNIX Simucad SilosIII simulator, and the UNIX Synopsys VCS simulator.

For specific information about which versions are supported with this release, go to the Guru automated technical support system on the Actel Web site (http://www.actel.com/guru) and type the following in the Keyword box:

```
third party
```

UNIX System Setup

After installing Designer, make sure the proper environment variables are set in your UNIX shell script. The following are C shell variables. If you are using another shell, adjust the syntax accordingly.

```
setenv ALSDIR <actel_install_directory>
set path=($ALSDIR/bin $path)
```

If you are using SunOS or Solaris, the following variable must also be set:

```
setenv LD_LIBRARY_PATH $ALSDIR/lib
```

If you are using HP-UX, the following variable must also be set:

```
setenv SHLIB_PATH $ALSDIR/lib
```

Refer to the *Designing with Actel* manual and the documentation included with your simulation tool for additional information about setting environment variables.

Verilog Libraries

The Actel Verilog libraries contain Verilog models for each Actel macro in all Actel families. The Verilog libraries are installed in the "<actel_install_directory>/lib/vlog/<act_fam>" directories.

Migration Libraries

In addition to the standard Actel libraries, Actel provides a set of migration libraries. These libraries contain macros that were supported in 3.1.1u1 and earlier versions of the Designer Series software and macros that may be needed to retarget designs from a different Actel family. Actel does not recommend using the migration libraries on new designs. The Verilog migration libraries are installed in the "<actel_install_directory>/lib/vlog/<act_fam>_mig" directories.

Compiling Verilog Libraries

Before simulating a design with the MTI V-System, MTI ModelSim, or the Mentor Graphics QuickHDL Verilog simulator, you must compile the Actel Verilog libraries. This section describes the procedures. Refer to the documentation included with your simulation tool for additional information about compiling libraries.

MTI ModelSim and V-System Simulators

Use the following procedure to compile Verilog libraries for the MTI ModelSim and V-System simulators. UNIX commands are typed at the UNIX prompt. PC commands are typed on the command line of the MTI Transcript window. The commands shown are for PC. To make the commands work for UNIX, use forward slashes instead of back slashes

1. **Create a directory called "mti" in the "$ALSDIR\lib\vlog" directory.**
2. **Invoke the simulator (PC only).**
3. **Change to the "$ALSDIR\lib\vlog\mti" directory.** Type the following command:

   ```
   cd $ALSDIR\lib\vlog\mti
   ```

4. **Create an <act_fam> family library directory for the simulator.** Type the following command:

   ```
   vlib <act_fam>
   ```

5. **Compile the Actel library.** Type the following command:

   ```
   vlog -work <act_fam> $ALSDIR\lib\vlog\<act_fam>\*.v
   ```

6. **(Optional) Compile the Migration library.** Only perform this step if you are using the migration library. Type the following command:

   ```
   vlog -work <act_fam> $ALSDIR\lib\vlog\<act_fam>_mig\*.v
   ```

Mentor Graphics QuickHDL Simulator

Use the following procedure to compile Verilog libraries for the Mentor Graphics QuickHDL simulator.

1. **Create a directory called "qhdl" in the "$ALSDIR/lib/vlog" directory.**
2. **Change to the "$ALSDIR/lib/vlog/qhdl" directory.** Type the following command:

   ```
   cd $ALSDIR/lib/vlog/qhdl
   ```

3. **Create an <act_fam> family library directory for the simulator.** Type the following command:

   ```
   qhlib <act_fam>
   ```

4. **Compile the Actel family models.** Type the following command:

   ```
   qvlcom -work <act_fam> $ALSDIR/lib/vlog/<act_fam>/*.v
   ```

5. **(Optional) Compile the Migration library.** Only perform this step if you are using the migration library. Type the following command:

   ```
   qvlcom -work <act_fam> $ALSDIR/lib/vlog/<act_fam>_mig/*.v
   ```

2

Design Flow

This chapter illustrates and describes the design flow for creating Actel designs using Verilog simulation and the Designer Series software.

Actel-Verilog Design Flow Illustrated

Figure 2-1 shows the design flow for an Actel device using CAE software, a Verilog simulation tool, and the Designer Series software[1].

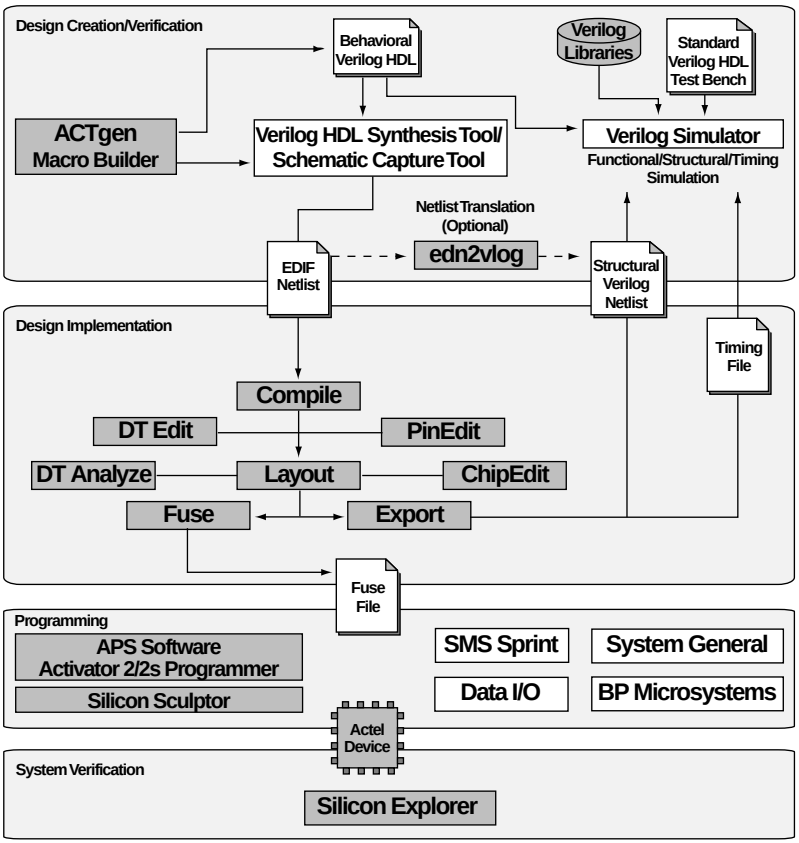

Figure 2-1. Actel-Verilog Design Flow

1. Actel-specific utilities/tools are denoted by the grey boxes in Figure 2-1.

Actel-Verilog Design Flow Overview

The Actel-Verilog design flow has four main steps; design creation/verification, design implementation, programming, and system verification. These steps are described in the following sections.

Design Creation/ Verification

During design creation/verification, a design is captured as a schematic or as an RTL-level (behavioral) Verilog HDL source file.

If your design is a Verilog HDL source file, a behavioral simulation can be performed to verify that the HDL code is correct. The code is then synthesized into an Actel gate-level (structural) Verilog HDL netlist. After synthesis, a structural simulation of the design can be performed. Finally, an EDIF netlist is generated for use in Designer and a structural Verilog netlist is generated for structural and timing simulation.

If your design is a schematic, an EDIF netlist is generated for use in Designer and a structural Verilog netlist is generated for structural and timing simulation. You do not perform behavioral simulation or synthesis.

Design Capture

Enter your schematic using a third-party schematic capture tool or create your Verilog HDL source file using a text editor or a context-sensitive HDL editor. Your Verilog HDL design source can contain RTL-level constructs as well as instantiations of structural elements, such as ACTgen macros. Refer to the documentation included with your design capture tool for information about design capture.

Behavioral Simulation

Perform a behavioral simulation of your design before synthesis. Behavioral simulation verifies the functionality of your Verilog HDL code. A standard Verilog HDL test bench can be used to drive simulation. Refer to “Behavioral Simulation” on page 12 and the documentation included with your simulation tool for information about performing functional simulation.

Synthesis

After you have created your Verilog HDL source file, you must synthesize it before placing and routing it in Designer. Synthesis transforms the Verilog HDL source file into a gate-level netlist and optimizes the design for a target technology. Refer to the documentation included with your synthesis tool for information about performing design synthesis.

EDIF Netlist Generation

After you have created, synthesized (if your design is an HDL source file), and verified your design, you must generate an EDIF netlist for place and route in Designer. If your design is a Verilog HDL source file, the EDIF netlist is also used to generate a structural Verilog netlist. Refer to "Generating an EDIF Netlist" on page 9 and the documentation included with your schematic capture or synthesis tool for information about generating an EDIF netlist.

Structural Verilog Netlist Generation

Generate a structural Verilog netlist from your EDIF netlist for use in structural and timing simulation by either exporting it from Designer or by using the Actel "edn2vlog" program. Refer to "Generating a Structural Verilog Netlist" on page 9 for information about generating a structural netlist.

Structural Simulation

Perform a structural simulation of your design before placing and routing it. Structural simulation verifies the functionality of your structural Verilog netlist. Default unit delays included in the Verilog libraries are used for every gate. Refer to "Structural Simulation" on page 13 and the documentation included with your simulation tool for information about performing structural simulation.

Design Implementation

During design implementation, a design is placed and routed using Designer. Additionally, static timing analysis can be performed on a design in Designer with the DT Analyze tool. After place and route, post-layout (timing) simulation is performed with a Verilog simulator.

Place and Route

Use Designer to place and route your design. Make sure to specify Verilog as the Naming Style when importing the EDIF netlist into Designer. Refer to the *Designing with Actel* manual for information about using Designer.

Static Timing Analysis

Use the DT Analyze tool in Designer to perform static timing analysis on your design. Refer to the *Designing with Actel* manual for information about using DT Analyze.

Timing Simulation

Perform a timing simulation of your design after placing and routing it. Timing simulation requires information extracted from Designer, which overrides default unit delays in the Actel Verilog libraries. Refer to "Timing Simulation" on page 14 and the documentation included with your simulation tool for information about performing timing simulation.

Programming

Program a device with programming software and hardware from Actel or a supported 3rd party programming system. Refer to the *Designing with Actel* manual and the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information about programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Explorer Quick Start* for information about using the Silicon Explorer.

3

Generating Netlists

This chapter describes the procedures for generating EDIF and structural Verilog netlists.

Generating an EDIF Netlist

After capturing your schematic or synthesizing your design, generate an EDIF netlist from your schematic capture or synthesis tool. The EDIF netlist is used for place and route in Designer. Refer to the documentation included with your schematic capture or synthesis tool for information about generating an EDIF netlist.

Make sure to specify Verilog for the naming style when importing the EDIF netlist into Designer.

Generating a Structural Verilog Netlist

You can generate structural Verilog netlist using Designer or the "edn2vlog" program. The structural Verilog netlist is used for structural and timing simulation.

To generate a structural Verilog netlist using Designer:

1. **Invoke Designer.**
2. **Import the EDIF netlist.** Choose the Import Netlist File command from the File menu. The Import Netlist dialog box is displayed. Specify EDIF as the Netlist Type, GENERIC as the Edif flavor, and Verilog as the Naming Style. Type the full path name of your EDIF netlist or use the Browse button to select your design. Click OK.
3. **Export a structural Verilog netlist.** Choose the Export command from the File menu. The Export dialog box is displayed. Specify Netlist File as the File Type and Verilog as the Format. Click OK.

To generate a structural netlist using edn2vlog:

1. **Change to the directory that contains the EDIF netlist.**
2. **Type the following command at the UNIX or DOS prompt:**

```
edn2vlog FAM:{<act_fam>}
[ EDNIN:<EdifFile1>{+<EdifFile2...>} ]
[ VLGOUT:<Verilog_File> ]
[ SIMTEMP:<Stimulus_template_file> ]
<design_name>
```

The “EDNIN” option specifies the EDIF input file(s). You can specify multiple files with the “+” delimiter between file names. The default EDIF input file is <design_name>.edn. The “VLOGOUT” option specifies the Verilog output file names. The default Verilog output file is <design_name>.v. The “SIMTEMP” option instructs the program to generate a Verilog stimulus template file. If you do not specify this option, the program does not generate a stimulus file.

4 Interpreted Simulation

This chapter describes the procedures for performing functional (behavioral and structural) and timing simulation on an Actel design using tools that either interpret library and design files, or compile them on-the-fly. Cadence Verilog-XL, Simucad SilosIII, and Synopsys VCS are simulators in this category.

Also included in this chapter is information about creating a test bench and information about creating a command file to run a simulation in batch mode. Finally, some common Verilog simulation switches are described. Refer to the documentation included with your simulation tool for additional information about test benches, command files, switches, and performing simulation.

Creating a Test Bench

You can use a test bench to apply test vectors or patterns to a design during simulation to compare input and output patterns. The file can instantiate the top level design, using a Verilog pre-defined command, such as "$readmemb," "$monitor," and "$display." The test bench must be in the current project directory to be used. The following is an example test bench:

```
'timescale 1ns/100ps
module test;
//Inputs and outputs declaration
wire ............
reg ..................
//Instantiate the top module of your design in the test module
<top_module> <instance_name> (.....Pin List...);
...........
//stimulus patterns
initial
begin
.....
end
endmodule
```

Creating a Command File

You can use a command file for batch simulation. Your command file should include all command variables and Verilog switches you want to set during simulation. The following is an example command file:

```
<test_bench>.v
<design_name>.v
<verilog_switch_1> ... <verilog_switch_n>
```

The <design_name>.v variable is the Verilog top level design that includes all design sub-levels. This variable can represent a behavioral Verilog design for function simulation, or gate level Verilog design for structural or timing simulation.

The <verilog_switch_1> and <verilog_switch_n> variables represent Verilog switches that you can add to your command line during simulation. Refer to "Verilog Switches" on page 17 for information about available Verilog switches.

Behavioral Simulation

Use the following procedure to perform a behavioral simulation of a design. Refer to the documentation included with your simulation tool for additional information about performing behavioral simulation.

1. **Create or modify the test bench.** Make sure your test bench has a timescale definition added to it. The following is an example timescale definition:

   ```
   'timescale 1ns/100ps
   ```

   Refer to "Creating a Test Bench" on page 11 for information about creating test benches.

2. **Create or modify the command file.** A command file is only necessary if you are running batch simulation. Refer to "Creating a Command File" on page 12 for information.

3. **Simulate the design.** If your design is a Verilog HDL design, make sure that you simulate your behavioral Verilog HDL source file. Invoke the Verilog simulator by typing the following command:

```
<verilog_executable> <test_bench>.v <design_name>.v -y
$ALSDIR/lib/vlog/<act_fam> +libext+.v
```

If you are using the migrations libraries, type the following command:

```
<verilog_executable> <test_bench>.v <design_name>.v -y
$ALSDIR/lib/vlog/<act_fam> -y $ALSDIR/lib/vlog/<act_fam>_mig
+libext+.v
```

The "-y" and "+libtext+" options are Verilog switches that you can add to your command line during simulation. Refer to "Verilog Switches" on page 17 for information.

To simulate a design using a command file

Invoke the Verilog simulator by typing the following command:

```
<verilog_executable> -f <command_file>
```

The "-f" switch is necessary if you are using a command file to simulate a design.

Structural Simulation

Use the following procedure to perform a structural simulation on a design. Refer to the documentation included with your simulation tool for additional information about performing structural simulation.

1. **Create or modify the test bench.** Make sure your test bench has a timescale definition added to it. The following is an example timescale definition:

   ```
   'timescale 1ns/100ps
   ```

   Refer to "Creating a Test Bench" on page 11 for information about creating test benches.

2. **Create or modify the command file.** A command file is only necessary if you are running batch simulation. Refer to "Creating a Command File" on page 12 for information.

3. **Simulate the design.** If your design is a Verilog HDL design, make sure that you simulate your structural Verilog HDL netlist that you

generated using Designer or the "edn2vlog" program. Invoke the Verilog simulator by typing the following command:

```
<verilog_executable> <test_bench>.v <design_name>.v -y $ALS-
DIR/lib/vlog/<act_fam> +libext+.v
```

If you are using the migrations libraries, type the following command:

```
<verilog_executable> <test_bench>.v <design_name>.v -y $ALS-
DIR/lib/vlog/<act_fam> -y $ALSDIR/lib/vlog/<act_fam>_mig
+libext+.v
```

The "-y" and "+libtext+" options are Verilog switches that you can add to your command line during simulation. Refer to "Verilog Switches" on page 17 for information.

To simulate a design using a command file

Invoke the Verilog simulator by typing the following command:

```
<verilog_executable> -f <command_file>
```

The "-f" switch is necessary if you are using a command file to simulate a design.

Timing Simulation

Use the following procedure to perform a timing simulation on a design. Refer to the documentation included with your simulation tool for additional information about performing timing simulation.

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about placing and routing a design using Designer.
2. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a <design_name>.sdf file by choosing the SDF option from the CAE pull-down menu. Click OK.

3. **Create or modify a test bench.** Make sure your test bench has an "sdf_annotate" construct in it. The following is an example test bench with a construct line:

```
‘timescale 1ns/100ps
module test;

//Inputs and outputs declaration
wire ............
reg ..................

//Instantiate the top module of your design in the test mod-
ule
<top_module> <instance_name> (.....Pin List...);
...........

//stimulus patterns
initial
begin
.....
end

//Invoke SDF routine to back annotate
initial
$sdf_annotate(“<design_name>.sdf”,<instance_name>);
endmodule
```

   The "<instance_name>" variable is the top level instance name.

   Refer to "Creating a Test Bench" on page 11 for information about creating test benches.

4. **Create or modify the command file.** A command file is only necessary if you are running batch simulation. Refer to "Creating a Command File" on page 12 for information about creating command files.

5. **(VCS Only) Create a PLI table.** The PLI table is a text file that contains PLI commands for VCS. The following is an example PLI table called "sdf.tab" that uses the module "test" in the test bench example in step 3.

```
$sdf_annotate call=sdf_annotate_call
acc+=tchk,mp,mip,prx:test+
```

   Refer to the VCS documentation for information about creating a PLI table.

6. **Simulate the design.** If your design is a Verilog HDL design, make sure that you simulate your structural Verilog HDL netlist that you

generated using Designer or the “edn2vlog” program. Invoke the Verilog simulator by typing the following command:

VCS

```
vcs <test_bench>.v <design_name>.v -y $ALSDIR/lib/vlog/
<act_fam> +libext+.v -M -P sdf.tab
```

If you are using the migrations libraries, type the following command:

```
vcs <test_bench>.v <design_name>.v -y $ALSDIR/lib/vlog/
<act_fam> -y $ALSDIR/lib/vlog/<act_fam>_mig +libext+.v -M -P
sdf.tab
```

Other Simulators

```
<verilog_executable> <test_bench>.v <design_name>.v -y $ALS-
DIR/lib/vlog/<act_fam> +libext+.v
```

If you are using the migrations libraries, type the following command:

```
<verilog_executable> <test_bench>.v <design_name>.v -y $ALS-
DIR/lib/vlog/<act_fam> -y $ALSDIR/lib/vlog/<act_fam>_mig
+libext+.v
```

The “-y” and “+libtext+” options are Verilog switches that you can add to your command line during simulation. Refer to “Verilog Switches” on page 17 for information.

To simulate a design using a command file

Invoke the Verilog simulator by typing the following command:

```
<verilog_executable> -f <command_file>
```

The “-f” switch is necessary if you are using a command file to simulate a design.

Verilog Switches

This section defines and gives usage examples of some common Verilog switches for simulators that interpret design files or compile the files on-the-fly. Refer to the documentation included with your Verilog simulation tool for additional information about using switches during simulation.

Minus Switches

Table 4-1 defines and gives usage examples of Verilog minus switches:

Table 4-1. Minus Switches

Switch	Definition
-s	Stop option; initiates entry into interactive mode after successful design compilation.
-a	Accelerated option; directs accelerated, declared elements to be simulated in accelerated mode (Verilog-XL only).
-c	Compile only option; compiles the text code in data file and exits the simulation mode.
-d	Decompile option; retargets data files into existing text files.
-f	Command argument file option; reads invocation command from a text file.
-l	Log file option.
-y	Library directory option; specifies a target library directory.

Plus Switches

Table 4-2 defines and gives usage examples of Verilog plus switches:

Table 4-2. Plus Switches

Switch	Definition
+libext+	Used with -y switch.
+delay_mode_path	Specifies the path delay model for simulation.
+delay_mode_unit	Specifies the unit delay model for simulation.
+delay_mode_zero	Functional simulation option; specifies the zero delay model for simulation.
+mindelays	Back annotation option; selects minimum delay for simulation.
+maxdelays	Back annotation option; selects maximum delay for simulation.
+typdelays	Back annotation option; selects typical delay for simulation.

5
Simulation with MTI V-System or ModelSim

This chapter describes the procedures for performing functional (behavioral and structural) and timing simulation on an Actel design using commands for the Model Technology V-System or ModelSim simulator. Refer to the documentation included with your simulation tool for information about simulating a design using the graphical user interface.

Behavioral Simulation

Use the following procedure to perform a behavioral simulation of a design using the MTI V-System or ModelSim simulator. UNIX commands are typed at the UNIX prompt. PC commands are typed on the command line of the MTI Transcript window. The commands shown are for PC. To make the commands work for UNIX, use forward slashes instead of back slashes.

1. **Invoke the simulator (PC only).**
2. **Change directory to your project directory.** This directory must include your Verilog design files and test bench. Type the following command:

   ```
   cd <project_dir>
   ```

3. **Create a "work" directory.** Type the following command:

   ```
   vlib work
   ```

4. **Compile your design source and test bench file(s).** Before simulating your design, you must compile the source files and test bench. For hierarchical designs, compile the lower level design blocks before the higher level design blocks. Type the following commands:

   ```
   vlog <behavioral_design_file>.v
   vlog <test_bench>.v
   ```

5. **Simulate your design.** Type the following command:

   ```
   vsim <topmost_module_name>
   ```

For example:

```
vsim test_adder_behave
```

The module test_adder_behave in the test bench will be simulated.

If any Actel macros are instantiated in your Verilog source, use the following command to simulate your design with compiled Actel Verilog library.

```
vsim -L $ALSDIR\lib\vlog\mti\<act_fam> <topmost_module_name>
```

Structural Simulation

Use the following procedure to perform a structural simulation of a design using the MTI V-System or ModelSim simulator. UNIX commands are typed at the UNIX prompt. PC commands are typed on the command line of the MTI Transcript window. The commands shown are for PC. To make the commands work for UNIX, use forward slashes instead of back slashes.

1. **Invoke the simulator (PC only).**
2. **Change directory to your project directory.** This directory must include your Verilog design files and test bench. Type the following command:

   ```
   cd <project_dir>
   ```

3. **Create a "work" directory.** You only need to create a work directory if you are using a different project directory than the one you used for behavioral simulation. Type the following command:

   ```
   vlib work
   ```

4. **Compile the structural netlist and test bench.** If you have not already generated a structural Verilog netlist, go to "Generating a Structural Verilog Netlist" on page 9 for the procedure. Type the following commands:

   ```
   vlog <structural_netlist>.v
   vlog <test_bench>.v
   ```

5. **Simulate your design.** Type the following commands:

   ```
   vsim -L $ALSDIR\lib\vlog\mti\<act_fam> <topmost_module_name>
   ```

   For example:

   ```
   vsim -L $ALSDIR\lib\vlog\mti\42mx test_adder_structure
   ```

   The module test_adder_structure in the test bench will be simulated using the compiled 42MX Verilog library.

Timing simulation

Use the following procedure to perform a timing simulation of a design using the MTI V-System or ModelSim simulator. UNIX commands are typed at the UNIX prompt. PC commands are typed on the command line of the MTI Transcript window. The commands shown are for PC. To make the commands work for UNIX, use forward slashes instead of back slashes.

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about placing and routing a design using Designer.
2. **Extract timing information for your design from Designer.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog is displayed. Create a <design_name>.sdf file by choosing the SDF option from the CAE pull-down menu. Click OK.
3. **Invoke the simulator (PC only).**
4. **Change directory to your project directory.** This directory must include your Verilog design files and test bench. Type the following command:

   ```
   cd <project_dir>
   ```

5. **Create a "work" directory.** You only need to create a work directory if you are using a different project directory than the one you used for behavioral and structural simulation. Type the following command:

```
vlib work
```

6. **Compile the structural netlist and test bench.** If you have not already generated a structural Verilog netlist, go to "Generating a Structural Verilog Netlist" on page 9 for the procedure. Type the following commands:

```
vlog <structural_netlist>.v
vlog <test_bench>.v
```

7. **Simulate your design using timing information contained in the SDF file.** Type the following command:

```
vsim -L $ALSDIR\lib\vlog\mti\<act_fam> -sdf[max|typ|min]
/<region>=<design name>.sdf -c <topmost_module_name>
```

The <region> option specifies the region (or path) to an instance in a design where back annotation begins. You can use it to specify a particular FPGA instance in a larger system design or testbench that you wish to back annotate. For example:

```
vsim -L $ALSDIR\lib\vlog\mti\42mx -sdfmax /uut=adder.sdf -c
test_adder_structural
```

In this example, the module "adder" has been instantiated as instance "uut" in the test bench. The module named "test_adder_structural" in the test bench will be simulated using the maximum delays specified in the SDF file.

6
Simulation with Mentor Graphics QuickHDL

This chapter describes the procedures for performing functional (behavioral and structural) and timing simulation on an Actel design using commands for the Mentor Graphics QuickHDL simulator. Refer to the documentation included with your simulation tool for information about simulating a design using the graphical user interface.

Behavioral Simulation

Use the following procedure to perform a behavioral simulation of a design using the Mentor Graphics QuickHDL simulator.

1. **Change directory to your project directory.** This directory must include your Verilog design files and test bench. Type the following command:

   ```
   cd <project_dir>
   ```

2. **Create a "work" directory.** Type the following command:

   ```
   qhlib work
   ```

3. **Compile your design source and test bench file(s).** Before simulating your design, you must compile the source files and test bench. For hierarchical designs, compile the lower level design blocks before the higher level design blocks. Type the following commands:

   ```
   qvlcom <behavioral_design_file>.v
   qvlcom <test_bench>.v
   ```

4. **Simulate your design.** Type the following command:

   ```
   qhsim <topmost_module_name>
   ```

   For example:

   ```
   qhsim test_adder_behave
   ```

   The module test_adder_behave in the test bench will be simulated.

If any Actel macros are instantiated in your Verilog source, use the following command to simulate your design with compiled Actel Verilog library.

```
qhsim -L $ALSDIR/lib/vlog/qhdl/<act_fam>
<topmost_module_name>
```

Structural Simulation

Use the following procedure to perform a structural simulation of a design using the Mentor Graphics QuickHDL simulator.

1. **Change directory to your project directory.** This directory must include your Verilog design files and test bench. Type the following command:

   ```
   cd <project_dir>
   ```

2. **Create a "work" directory.** You only need to create a work directory if you are using a different project directory than the one you used for behavioral simulation. Type the following command:

   ```
   qhlib work
   ```

3. **Compile the structural netlist and test bench.** If you have not already generated a structural Verilog netlist, go to "Generating a Structural Verilog Netlist" on page 9 for the procedure. Type the following commands:

   ```
   qvlcom <structural_netlist>.v
   qvlcom <test_bench>.v
   ```

4. **Simulate your design.** Type the following commands:

   ```
   qhsim -L $ALSDIR/lib/vlog/qhdl/<act_fam>
   <topmost_module_name>
   ```

   For example:

   ```
   qhsim -L $ALSDIR/lib/vlog/qhdl/42mx test_adder_structure
   ```

   The module test_adder_structure in the test bench will be simulated using the compiled 42MX Verilog library.

Timing simulation

Use the following procedure to perform a timing simulation of a design using the Mentor Graphics QuickHDL simulator.

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about placing and routing a design using Designer.
2. **Extract timing information for your design from Designer.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog is displayed. Create a <design_name>.sdf file by choosing the SDF option from the CAE pull-down menu. Click OK.
3. **Change directory to your project directory.** This directory must include your Verilog design files and test bench. Type the following command:

   ```
   cd <project_dir>
   ```

4. **Create a "work" directory.** You only need to create a work directory if you are using a different project directory than the one you used for behavioral and structural simulation. Type the following command:

   ```
   qhlib work
   ```

5. **Compile the structural netlist and test bench.** If you have not already generated a structural Verilog netlist, go to "Generating a Structural Verilog Netlist" on page 9 for the procedure. Type the following commands:

   ```
   qvlcom <structural_netlist>.v
   qvlcom <test_bench>.v
   ```

6. **Simulate your design using timing information contained in the SDF file.** Type the following command:

```
qhsim -L $ALSDIR\lib\vlog\qhdl\<act_fam> -sdf[max|typ|min]
/<region>=<design name>.sdf -c <topmost_module_name>
```

The <region> option specifies the region (or path) to an instance in a design where back annotation begins. You can use it to specify a particular FPGA instance in a larger system design or test bench that you wish to back annotate. For example:

```
qhsim -L $ALSDIR\lib\vlog\qhdl\42mx -sdfmax /uut=adder.sdf -
c test_adder_structural
```

In this example, the module “adder” has been instantiated as instance “uut” in the test bench. The module named “test_adder_structural” in the test bench will be simulated using the maximum delays specified in the SDF file.

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a Web and FTP site, electronic mail, and worldwide sales offices. This appendix contains information about using these services and contacting Actel for service and support.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel Toll-Free Line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4252 or +44 (0) 1256 305600.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Customer Applications Center

The Customer Applications Center is staffed by applications engineers who can answer your hardware, software, and design questions.

All calls are answered by our Technical Message Center. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 a.m. to 5 p.m., Pacific Standard Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

European customers can call +44 (0) 1256 305600.

Guru Automated Technical Support

Guru is a Web based automated technical support system accessible through the Actel home page (**http://www.actel.com/guru/**). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations and links to other resources on the Actel Web site. Guru is available 24 hours a day, seven days a week.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is **http://www.actel.com**. You are welcome to share the resources we have provided on the net.

Be sure to visit the "Actel User Area" on our Web site, which contains information regarding: products, technical services, current manuals, and release notes.

FTP Site

Actel has an anonymous FTP site located at **ftp://ftp.actel.com**. You can directly obtain library updates, software patches, design files, and data sheets.

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. The e-mail account is monitored several times per day.

The technical support e-mail address is **tech@actel.com**.

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