For:reese
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Document:Test 2
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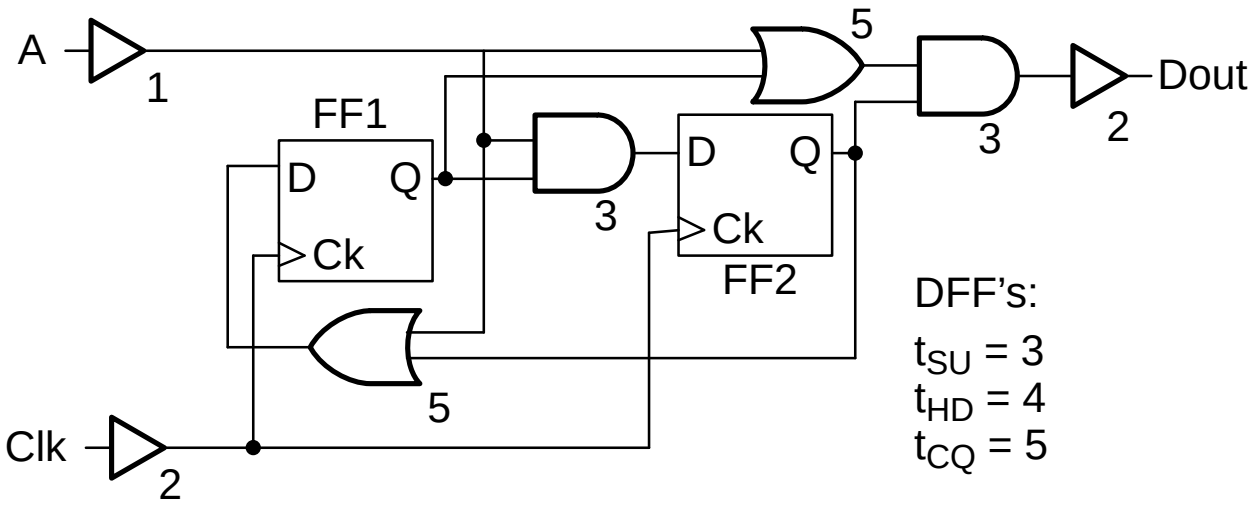
Test #2 – EE 4743 – Spring 1998 My Name is: _____

You have 50 minutes to complete this test. Good luck! Point values for ‘‘sub–questions’’ are indicated inside parentheses.

1. (30 points) Consider the diagram and answer the questions below. Delays for each gate are shown, in ns, next to each gate and delays for the flip–flops are shown in the table.



a. What is the longest register–to–register path? Based on that path, what is the fastest allowable clock cycle time?

b. What is the clock–to–output delay of Dout? Don’t forget to consider both possible paths!

c. True or false: The propagation delay of a flip–flop from D to Q is a very important circuit parameter. Why?

2. (35 points) Consider the equation below.

$$Y = 0.5\ Y@1 + 0.5\ X - X@1$$

a. Convert the equation to ‘‘shift–and–add’’ format.

b. Draw a flowgraph for it. Assume shifts are combinational.

c. What is the critical path? _____ The iteration loop critical path? _____

d. Use pipelining to reduce the critical path so that it is maximally pipelined. For maximum credit, use a *minimal* number of pipeline stages.

e. Estimate the amount of resources needed (for the flowgraph that you drew in part d) based on the total number of shifts and adds that are performed and the number of clock cycles.

Number of Adders: _____ Number of Shifters: _____

3. (35 points) Consider the flowgraph you drew in question 2b (the ***non–pipelined*** flowgraph that implemented the equation in question 2).
   a. Assign TASAP and TALAP pairs to the flowgraph. Assume the number of clock cycles per sample period equals the critical path. (Hint: You may want to redraw the graph below.)

   b. Schedule the flowgraph. Do not worry about amount of resources (for example, number of registers).

c. Draw a datapath that implements the flowgraph and schedule.

d. (BONUS) Create a table that shows the value of each datapath control signal on each clock cycle.