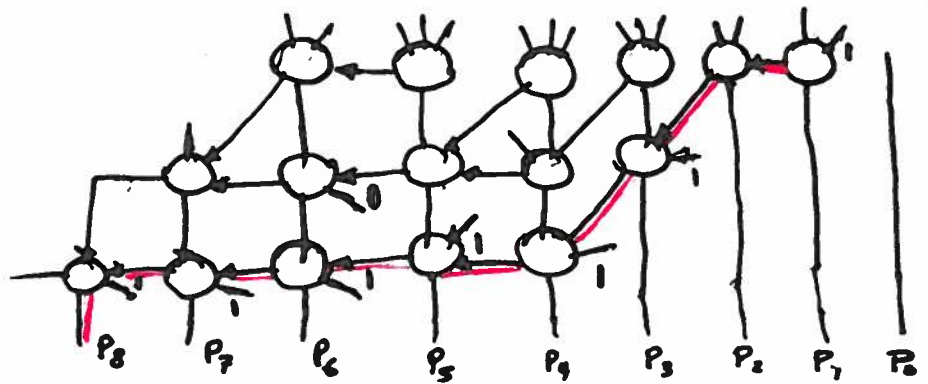


$$\begin{array}{r}
 5 = 0000101 \\
 \quad 1111010 \\
 \hline
 -5 \quad 1111011 \\
 \hline
 \end{array}$$

+ (-5)

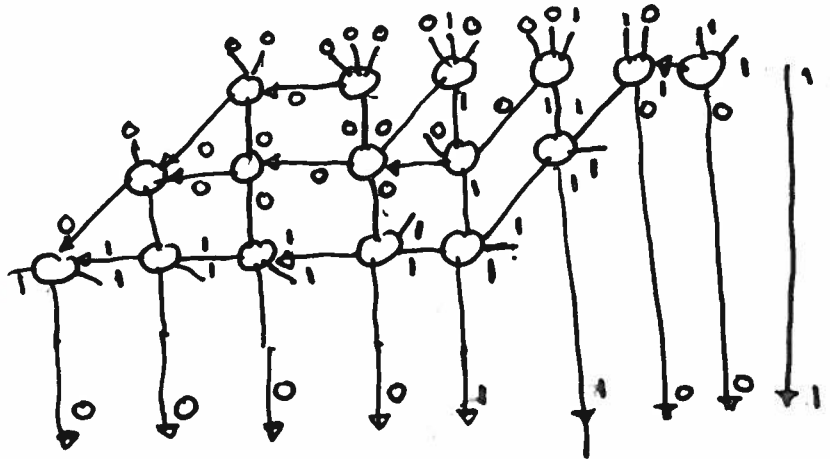
	x_3	x_2	x_1	x_0	y_3	y_2	y_1	y_0
	0	0	0	$x_3 y_0$	$x_2 y_0$	$x_1 y_0$	$x_0 y_0$	
	0	0	$x_3 y_1$	$x_2 y_1$	$x_1 y_1$	$x_0 y_1$		0
	0	$x_3 y_2$	$x_2 y_2$	$x_1 y_2$	$x_0 y_2$	0	0	0
$x_3 y_3$	$x_2 y_3$	$x_1 y_3$	$x_0 y_3$	0	0	0	0	0
	1	1	1	1	1	1	0	1



Architecture to calculate $2xy - 5$

To check

$$\begin{array}{r}
 5 \quad 0101 \\
 3 \quad 0011 \\
 \hline
 \quad \quad 0101 \\
 \quad \quad 0101 \\
 \quad \quad 0000 \\
 \quad \quad 0000 \\
 \hline
 3 \times 5 \quad 00001111 \\
 \hline
 2 \times 3 \times 5 \quad 000011110 \\
 \quad \quad 111111011 \\
 \hline
 2 \times 3 \times 5 - 5 \quad 000011001
 \end{array}$$



Checking with $x = 0101$ & $y = 0011$

Q2

$A = 7.25$, $M_A = 111.01_2$, $= 1.1101 \times 2^2$, $S_A = 0$, $e_A = 01111111 + 00000001$
 $B = -0.75$, $M_B = 0.11$, $= 1.10 \times 2^{-1}$, $S_B = 1$, $e_A = 10000001$
 $e_B = 01111111 - 00000000$
 $e_B = 01111110$

$A = \boxed{0 \ 1000 \ 0001 \ 1101 \ \dots \ 0}$
 $B = \boxed{1 \ 0011 \ 1110 \ 100 \ \dots \ 0}$

Exp A + Exp B - Bias

$$\begin{array}{r} \text{Exp A} \cdot 1000 \ 0001 \\ \text{Exp B} + 0111 \ 1110 \\ \hline 1111 \ 1111 \\ \text{bias} \leftarrow 1000 \ 0001 \\ \hline 1000 \ 0000 \end{array}$$

$$\begin{array}{r} 2' \text{ Complement of } 127 \\ 0111 \ 1111 \\ 1000 \ 0000 \\ \hline 1000 \ 0001 \end{array}$$

$$\begin{array}{r} A \times B : \quad 1.1101 \times \\ \quad \quad 1.1000 \\ \hline \quad \quad 11101 \\ \quad \quad 11101 \\ \hline 10.10111 \end{array}$$

$= \frac{1.010111}{= M_R} \times 2^1$ normalize exponent

new exponent $1000 \ 0000 + 0000 \ 0001 = 1000 \ 0001 = e_R$

Sign of Results $S_R = S_A \oplus S_B = 1 \oplus 0 = 1$

$\boxed{1 \ 1000 \ 0001 \ 01011100 \ \dots \ 0} \leftarrow A \times B$

Rounding methodology in IEEE 754 is to the nearest even. Advantage is assuming 50% occurrence of 0 or 1 then error is minimized. Disadvantage is extra hardware and the delay produced due to the add.

See notes for architecture

The rounding method is in accordance with the following Table

e	M	M ₀	R	S
---	---	----------------	---	---

add a "1" if the following condition is satisfied $R(M_0 + S)$

Significand	Rounding	error	Significand	Rounding	error
X0.00	X0	0	X1.00	X1	0
X0.01	X0	-1/4	X1.01	X1	-1/4
X0.10	X0	-1/2	X1.10	X1+1	+1/2
X0.11	X1	+1/4	X1.11	X1+1	+1/4

Q3 midterm 2015

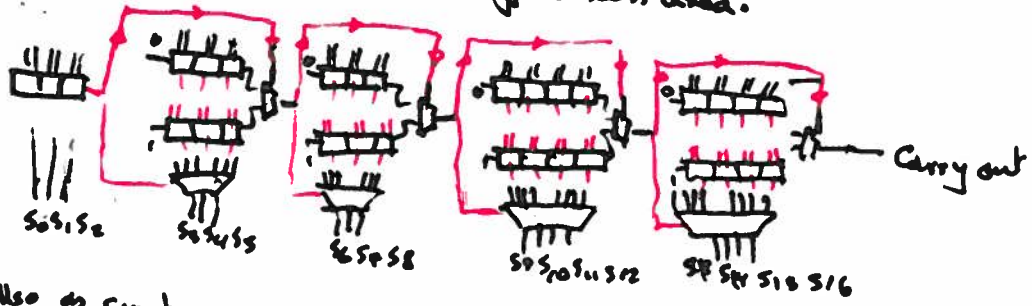
Advantage of carry save adders is its speed in comparison to other adders

Disadvantages are high area and power consumption. The best measures for Adders are its Delay-Power, DP or AT^2 where A is the area and T is the delay.

To make the 17-bit adder several alternative exist, some are listed below:
 assume $\tau_{MUX} = \frac{1}{2} \tau_{FA}$ c.e. delay of a 2:1 MUX is half of that of a Full Adder:

- | | | | |
|---|-----------------------------|--|-----------------------------|
| ① | 2 2 2 2 3 3 3 3 | $2 + \frac{6}{3} = 5 \tau_{FA}$ | - 32 FA + 21 MUX - Selected |
| ② | 3 3 3 4 4 4 | $3 + \frac{2}{2} = 5 \tau_{FA}$ | - 31 FA + 18 MUX |
| ③ | 4 4 4 5 | $5 + \frac{1}{2} = 5\frac{1}{2} \tau_{FA}$ | |
| ④ | 3 3 3 3 3 3 2 | $3 + \frac{5}{2} = 5\frac{1}{2} \tau_{FA}$ | |
| ⑤ | 5 6 6 1 | $6 + \frac{2}{2} = 7 \tau_{FA}$ | |

The selection also affect the amount of Full Adders and Muxes used. As shown ① and ② have the same delay but ① offers less area.



Also as can be seen complexity of the design has increased.