Designing Next-Generation DDR3-based Memory Interfaces

Agenda

- DDR3 timing margin challenges
- DDR3 features in Stratix® III FPGAs
- DDR3 smart interface module
- Timing closure tools
- Summary

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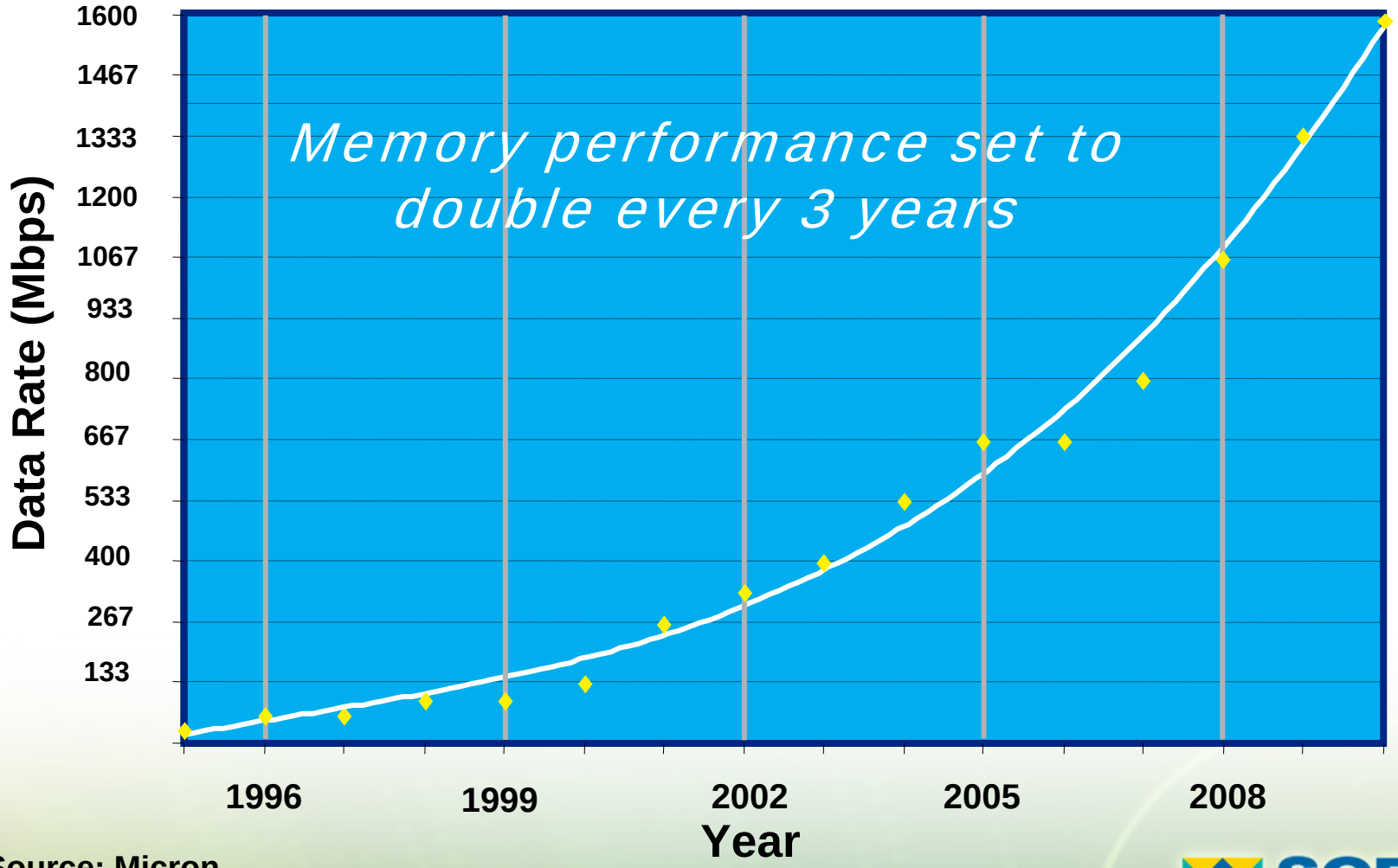
Mainstream Memory Trends



Source: Micron

DDR3 SDRAM Advantages

- Lower system power
  - DDR3 power: 30% to 40% lower than DDR2
  - FPGA Programmable Power Technology
- Higher density memories
  - Same board area
- Lower price over system lifetime
  - DDR3 price cross-over projected 2 years out
- Dynamic On-Chip Termination (OCT)
  - Proper line terminations and lower costs

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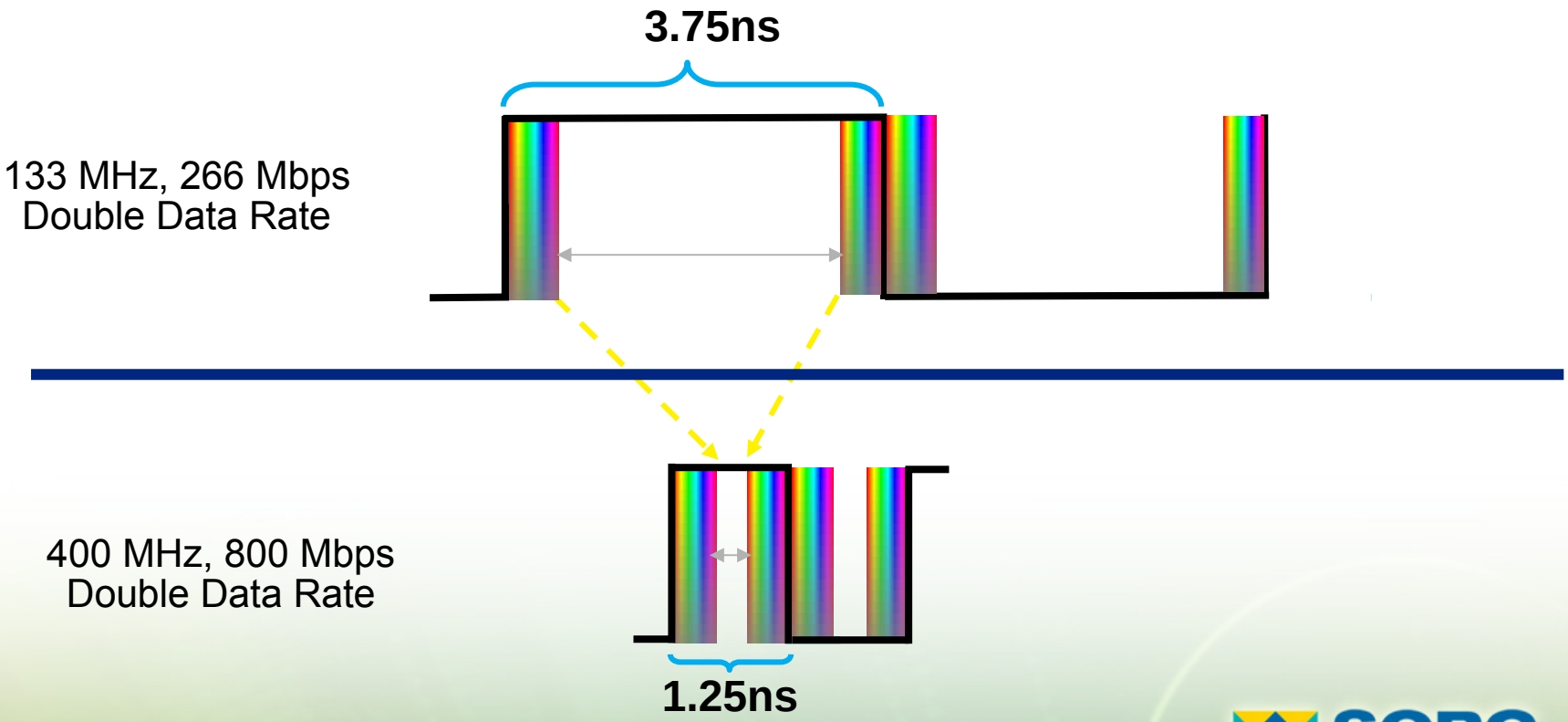
Timing Margin Challenges

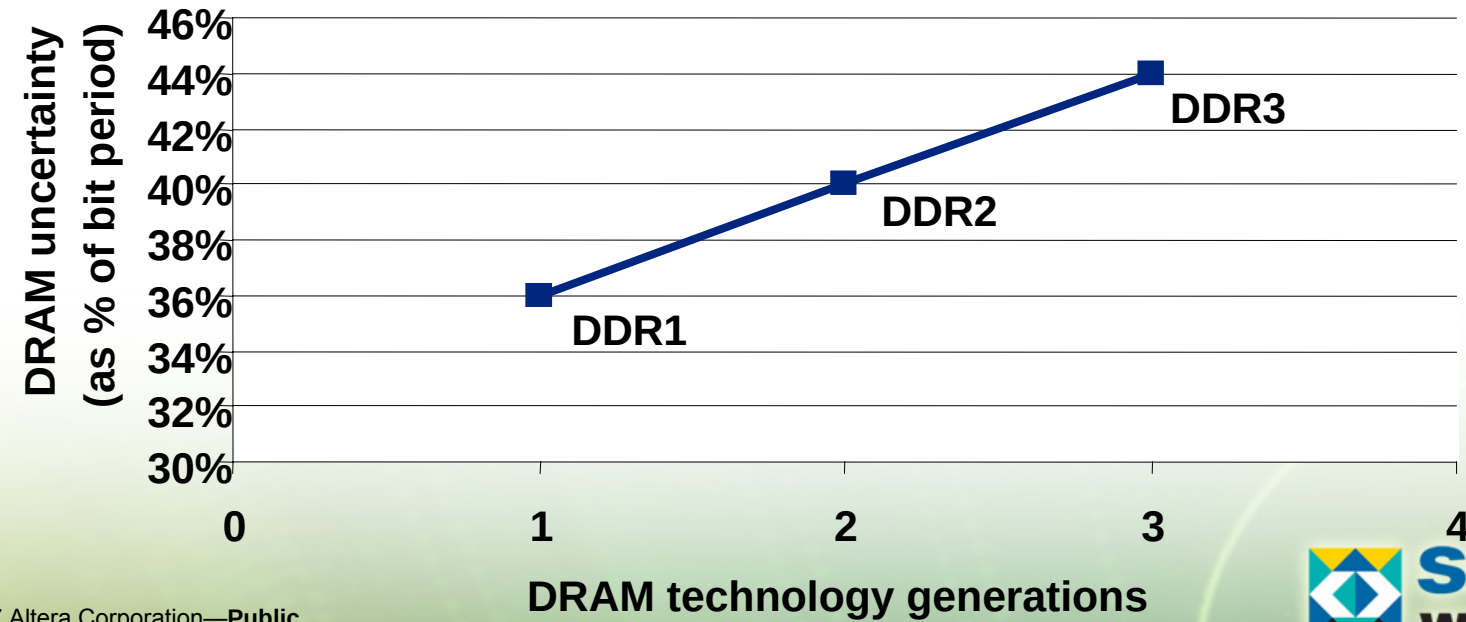
- Memory and board uncertainties do not scale with frequency
- Effects designers could previously ignore are now significant proportions of the cycle



Memory Uncertainty Increasing..

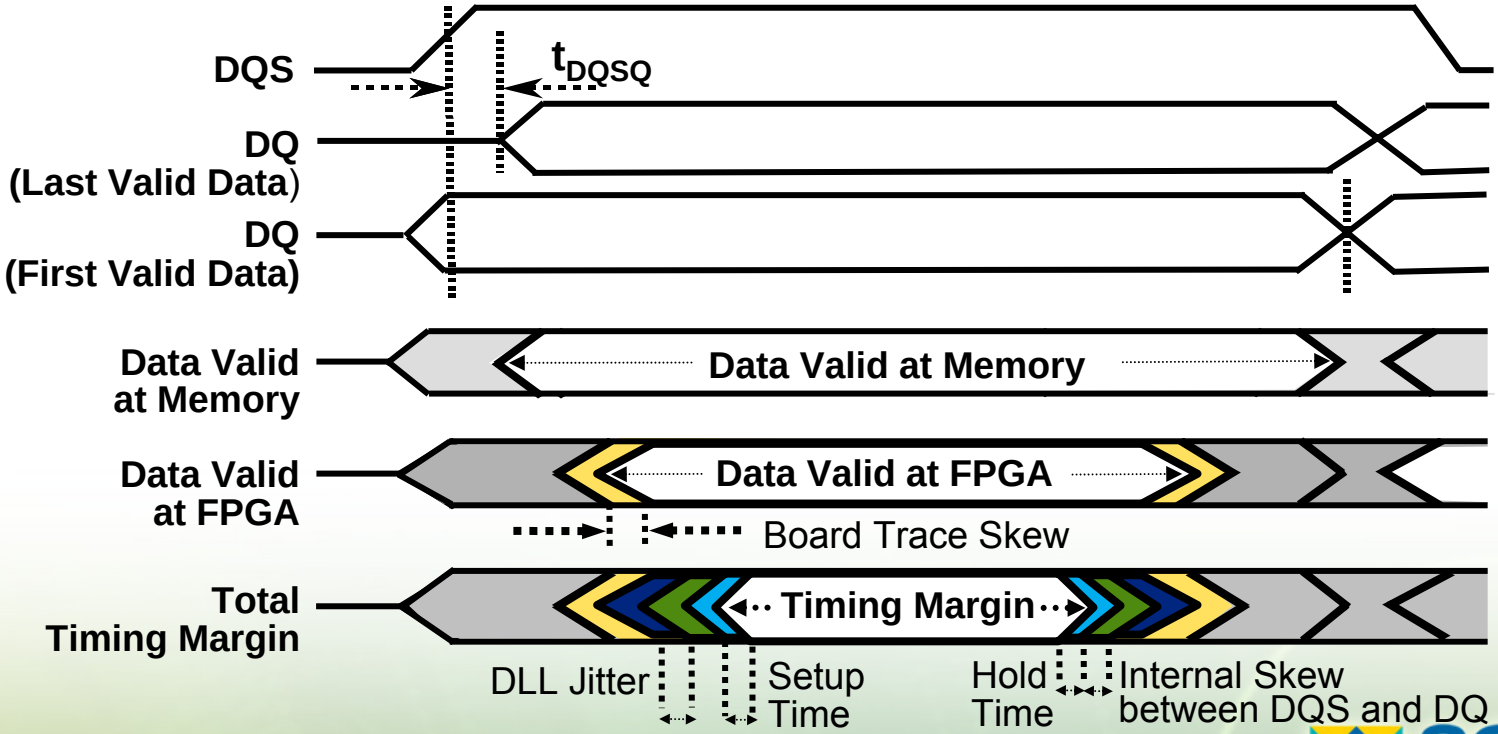
Memory parameters (ps)	DDR-400	DDR2-800	DDR3-800
t_{CK} clock period	5,000	2,500	2,500
Bit time	2,500	1,250	1,250
t_{DQSQ} DQS to DQ skew	400	200	200
t_{QH} data output hold time from DQS	2,000	950	900
Data eye at DRAM	1,600	750	700
% bit period	64%	60%	56%
DRAM uncertainties	**36%**	**40%**	**44%**

Source: Jedec



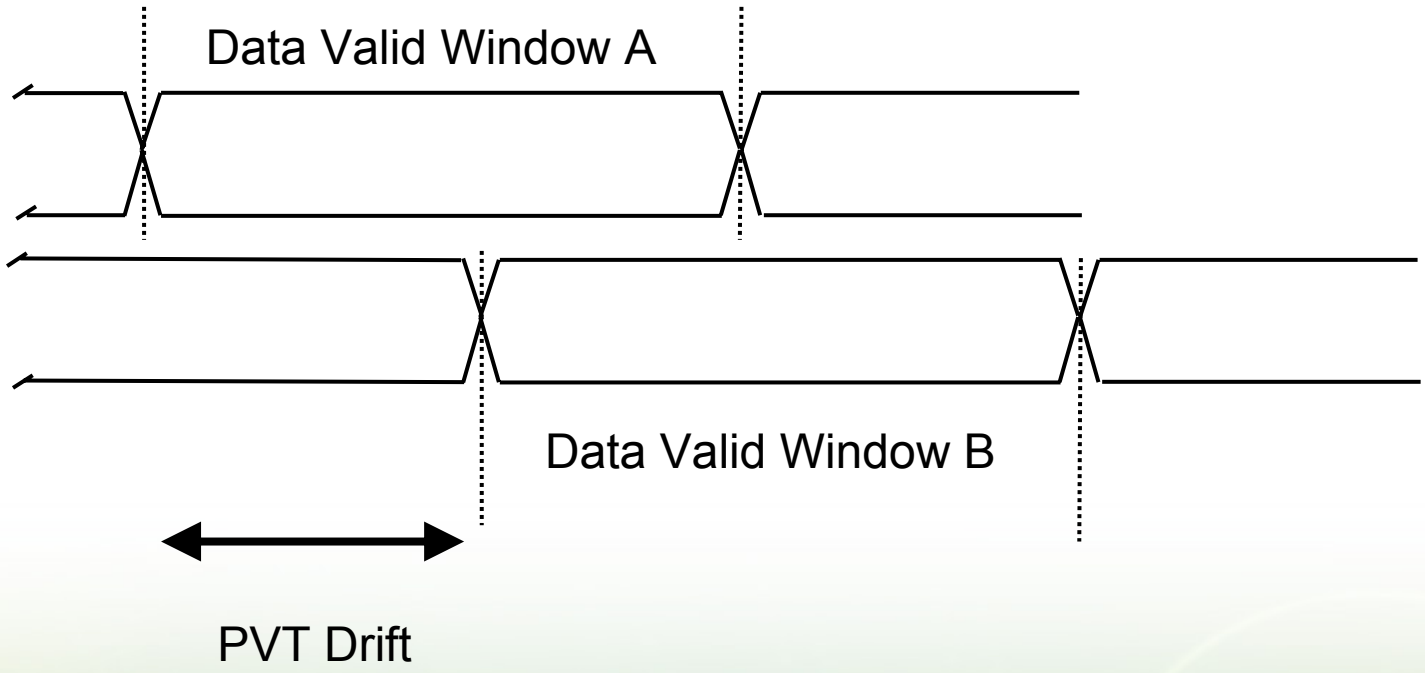
Shrinking Data Valid Window

- Following effects reduce the data valid window
  - The skew between first data valid and last data valid
  - Board trace skew
  - DLL jitter for DQS phase shift circuitry
  - Internal skew between DQS and DQ
  - Setup and hold time



Moving Data Valid Window

- Data valid window shifts with process, voltage, and temperature (PVT) variations



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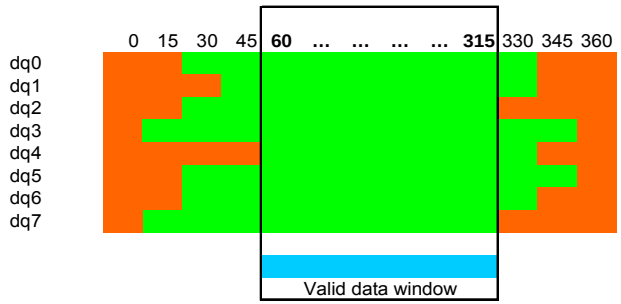
So how to tackle these challenges?

Some Techniques

Dynamic Calibration

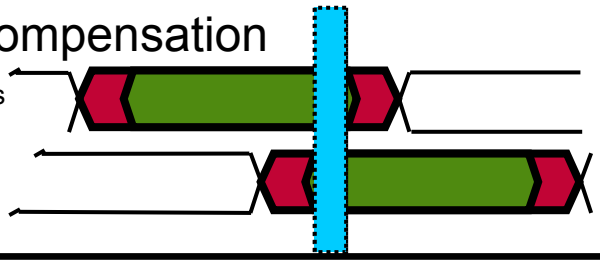
Without calibration: complex static timing analysis, narrow data valid window

With calibration: accurate strobe placement, wider data valid window

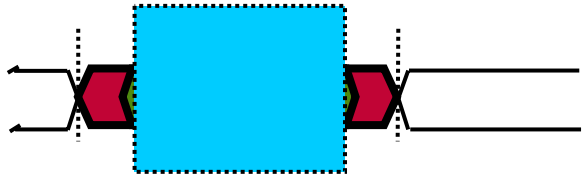


VT Compensation

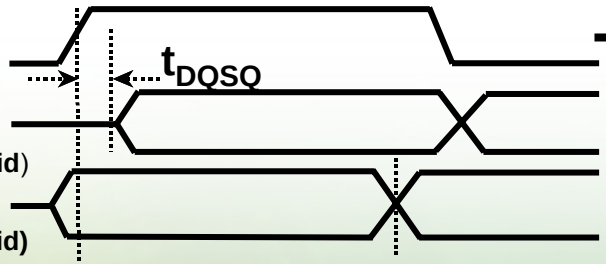
Data shifts due to VT variations



Voltage and temperature tracking

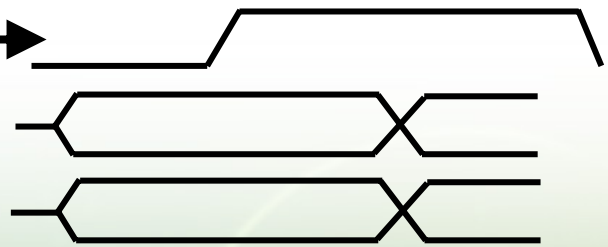


Deskew



DQS phase shift

Deskew



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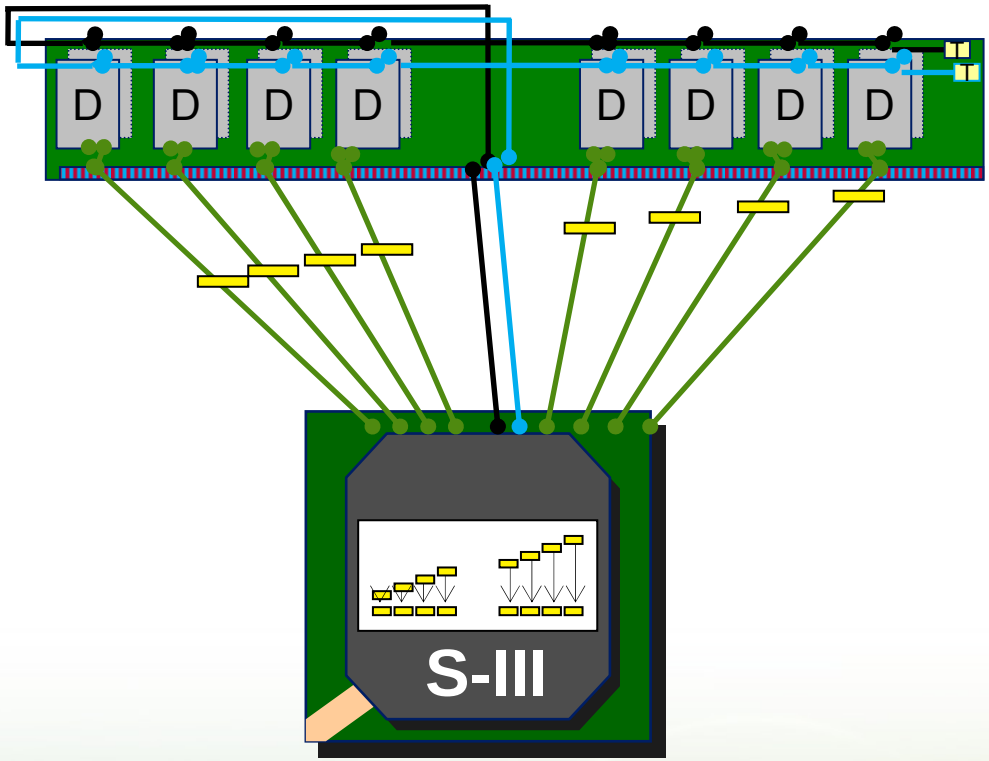
Leveling in DDR3 Interfaces

DDR3 Read-Write Leveling

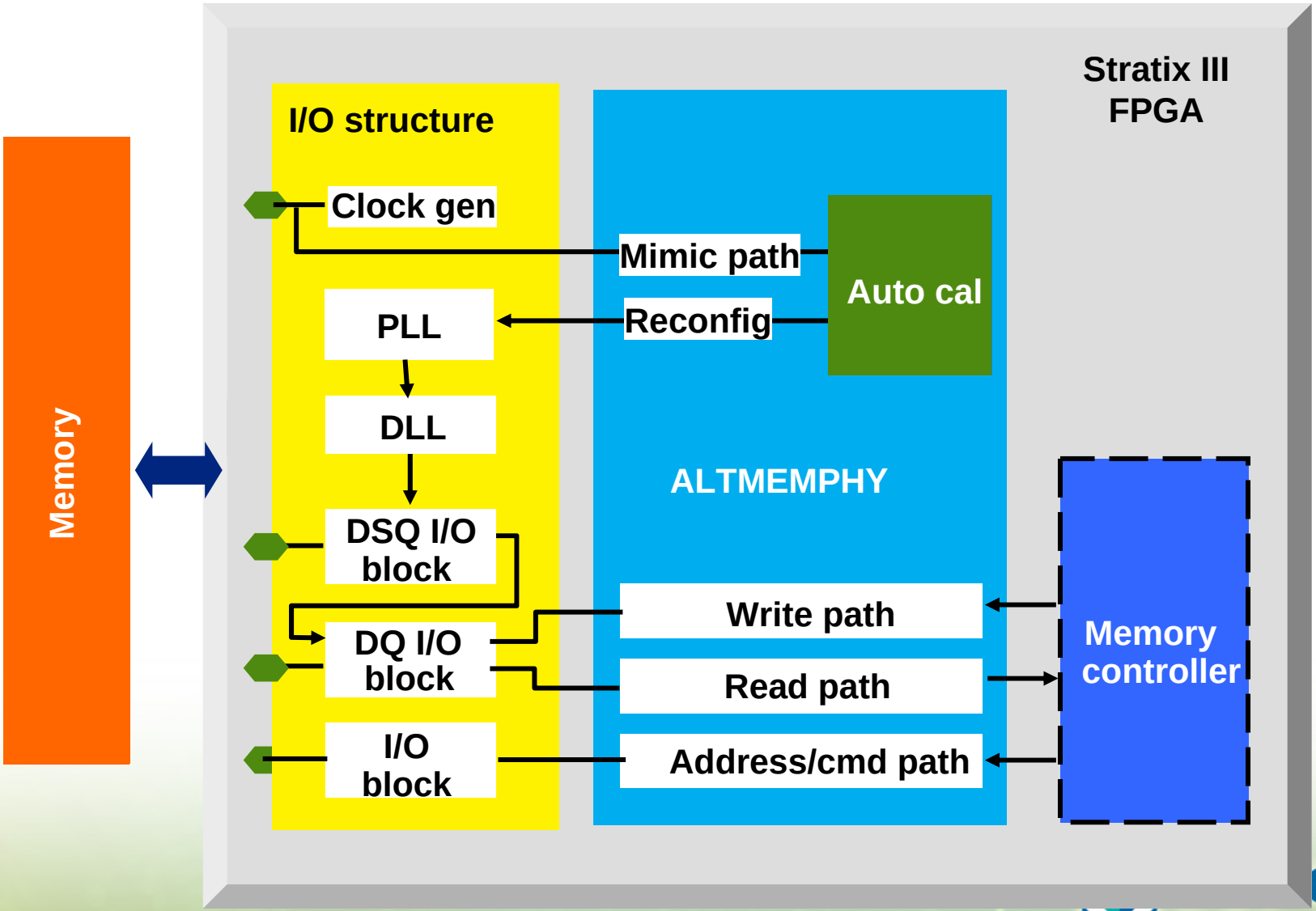
- Leveling
  - Required to compensate for DDR3 (Jedec) fly-by topology which causes flight time skew between CA/clock and DQS across a DIMM
- Write leveling
  - For writes, tDQSS at DRAM needs to be kept at ± 0.25 tCK
- Read leveling
  - Read data arrival time at memory controller could be spread over 2 clk cycles



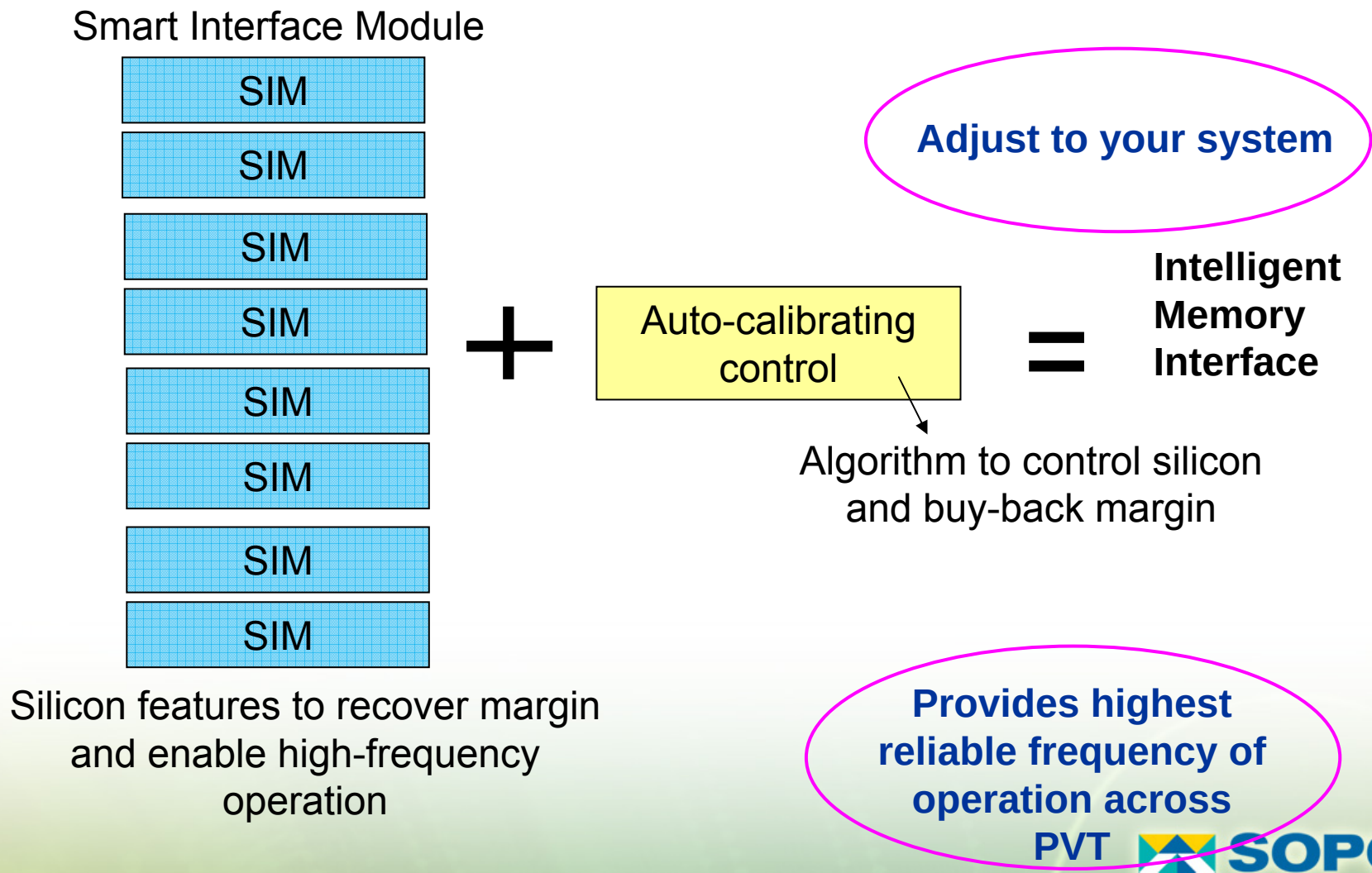
Courtesy: Qimonda

DDR3 Features in Stratix III FPGAs

DDR3 Smart Interface Module Using Stratix III FPGAs

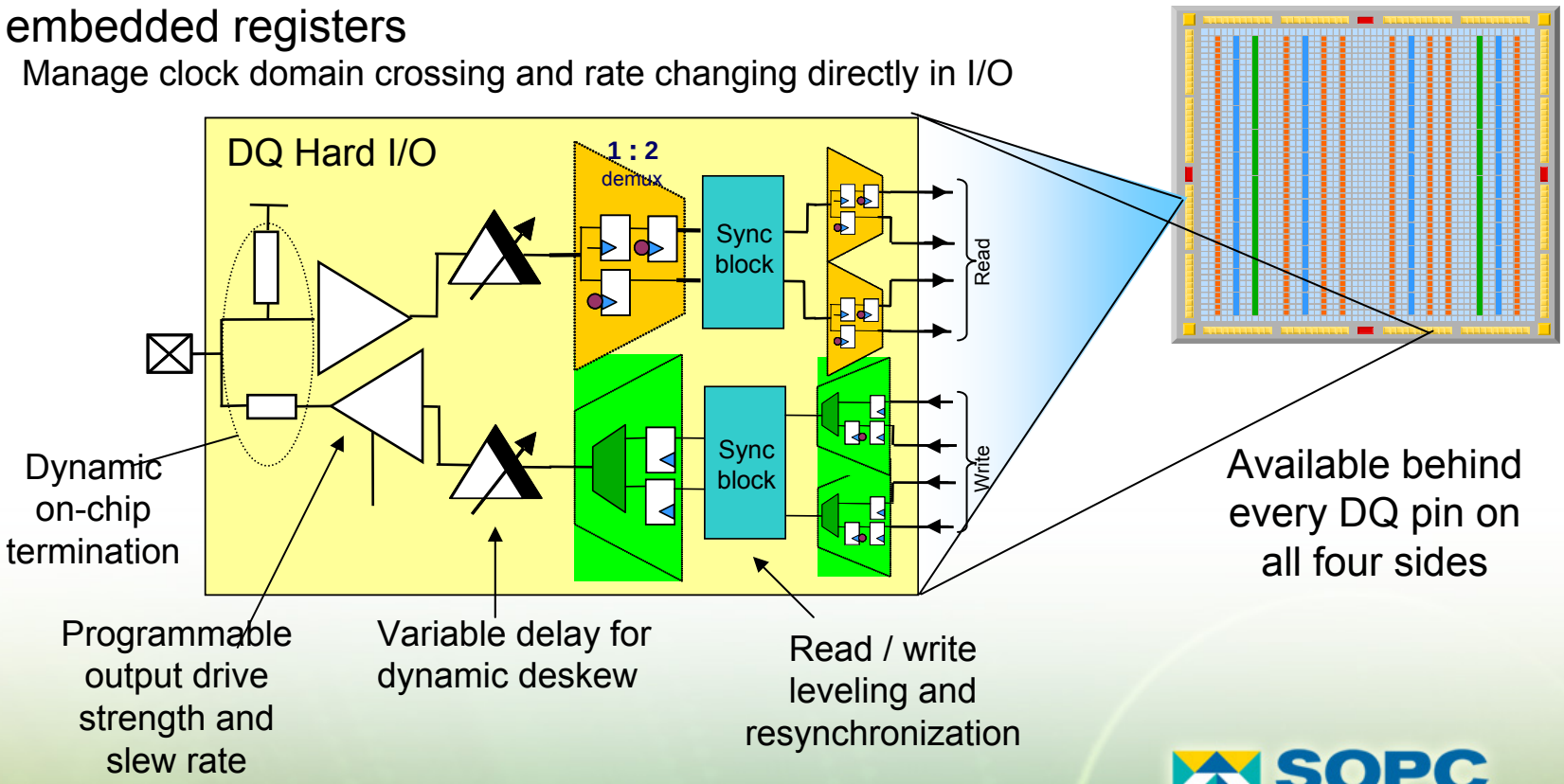


Smart Interface Module



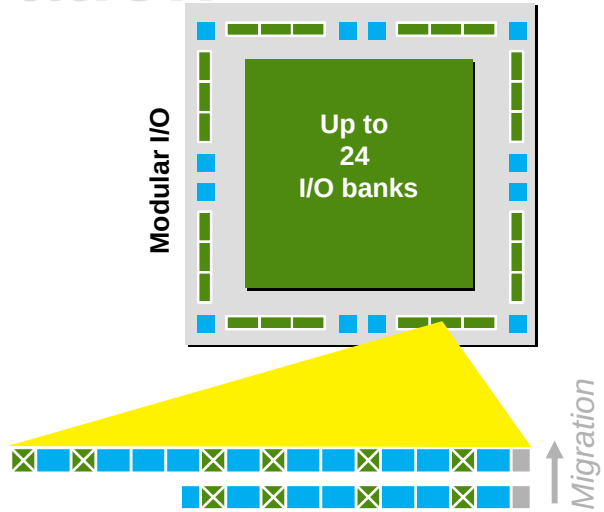
Stratix III DDR I/O Block

- Programmable I/O delay for deskew
- Controllable drive strength and slew rate for best-in-class signal integrity (SI)
- Half data rate option for design simplification
- Read / write leveling for DDR3 performance
- 31 embedded registers
  - Manage clock domain crossing and rate changing directly in I/O



Electricals And Vertical Migration

- Support over 40 I/O standards
- Mixed termination values in same bank
- New modular bank structure eases vertical migration
  - E.g. F1152 package identical for all family members over 8 die sizes



24- to 48-bit banks with common structure

9 Deep 8 Deep

	Device	484-Pin FBGA 1.0 mm 23 x 23	780-Pin FBGA 1.0 mm 29 x 29	1152-Pin FBGA 1.0 mm 35 x 35	1517-Pin FBGA 1.0 mm 40 x 40	1760-Pin FBGA 1.0 mm 43 x 43
Stratix III Logic	EP3SL50	288				
	EP3SL70					
	EP3SL110					
	EP3SL150					
	EP3SL200				864	
	EP3SE260					
	EP3SL340					1,104
Stratix III Enhanced	EP3SE50	288				
	EP3SE80					
	EP3SE110					
	EP3SE260				960	

Competitive FPGAs force you to re-spin board to get more logic

Differential I/O
Differential HSTL
Differential SSTL
Single-ended I/O
SSTL2, 18, 15 Class I and II
HSTL 18, 15, 12 Class I and II

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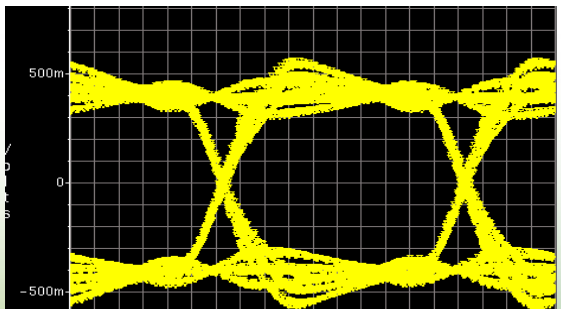
Pin Capacitance

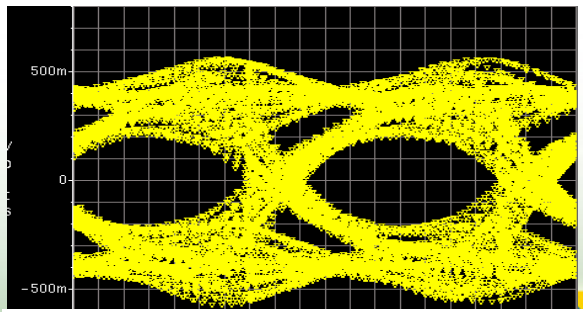
- Basic physics, pin capacitance matters
  - Higher capacitive loading = lower performance
    - Assume R = 50 ohm trace impedance

	Stratix III FPGA	Stratix II FPGA	Virtex 5 FPGA	Virtex 4 FPGA
Vertical I/O pin capacitance	5 pf	5 pf	9 pF	12 pF
Low pass filter - 3dB point	637 MHz	637 MHz	353 MHz	265 MHz

  - Skew and jitter uncertainties will reduce this number further
    - However, low pin cap and high toggle rates are mandatory for high performance
- Affect of pin capacitance in action



Stratix II FPGA



Stratix II FPGA with x2 pin cap deliberately added

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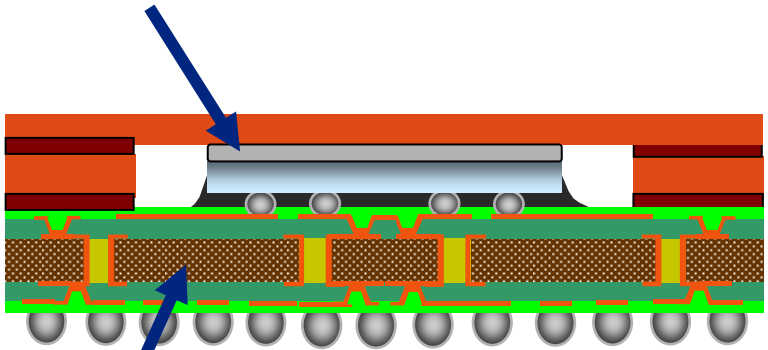
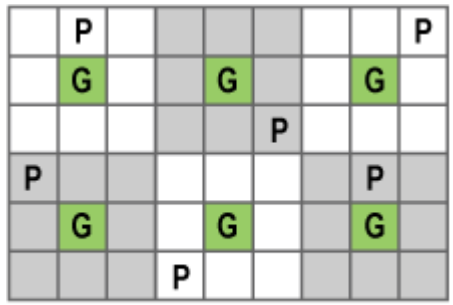
Die, Package, and Digital SI Enhancements

Significant silicon features	Benefits
■ Adjustable slew rate control (4 settings) ■ Advanced on-chip termination NEW! ■ User staggered output delay control ■ On-die capacitors NEW!	■ Reduce $\partial i/\partial t$ ■ Proper termination ■ Reduces simultaneous switching noise (SSN) ■ Improve power distribution network (PDN) quality



8:1:1 I/O:GND:PWR



In practise closer to 7:1:1

Significant package features	Benefits
■ On-package decoupling capacitors NEW! ■ 8:1:1 – I/O:GND:PWR ratio NEW! – Max distance between I/O and gnd = 1	■ Reduces loop inductance → reduces SSN ■ Improve PDN quality

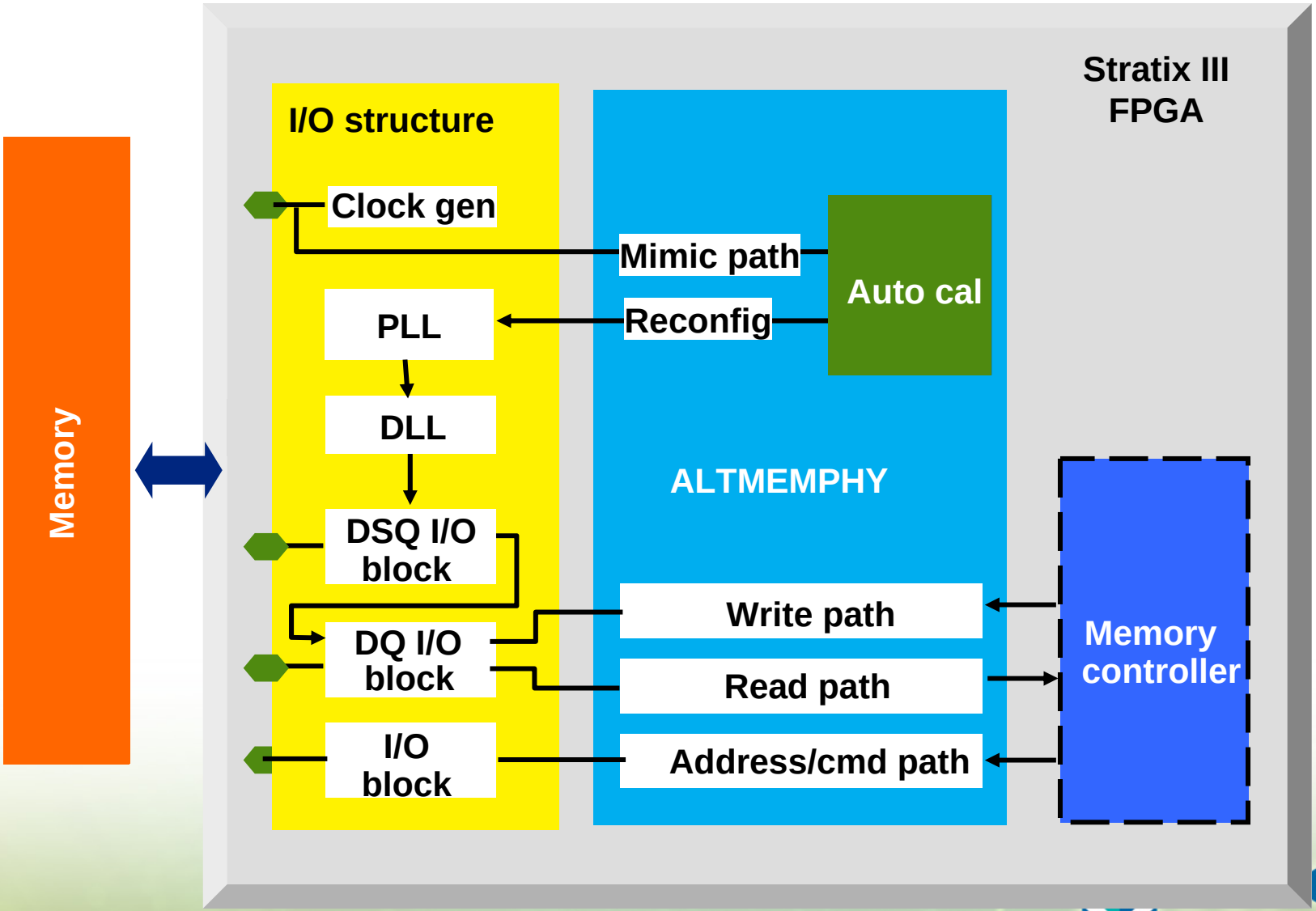
Calibration and Tracking

Dynamic Calibration

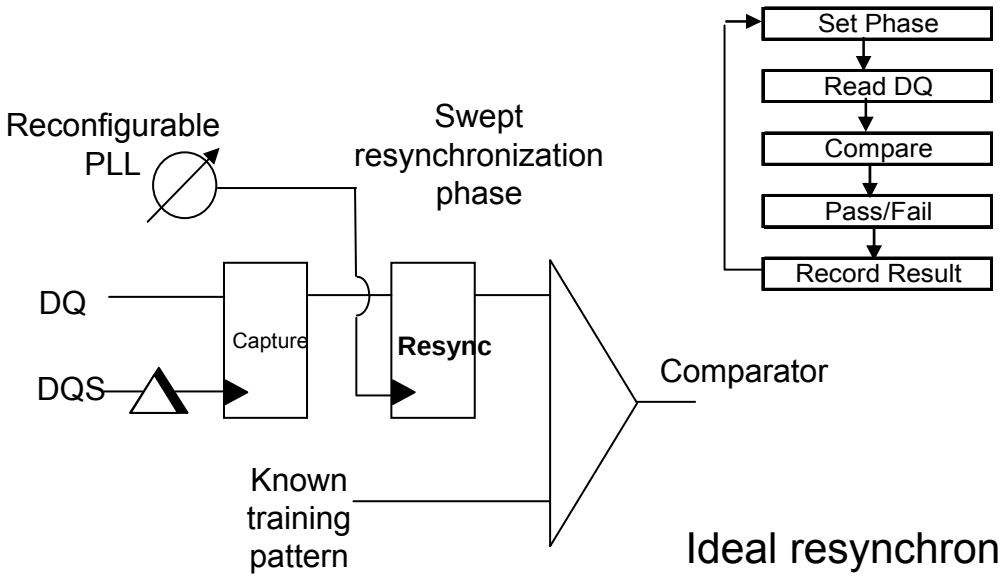
Timing margin based on static timing analysis

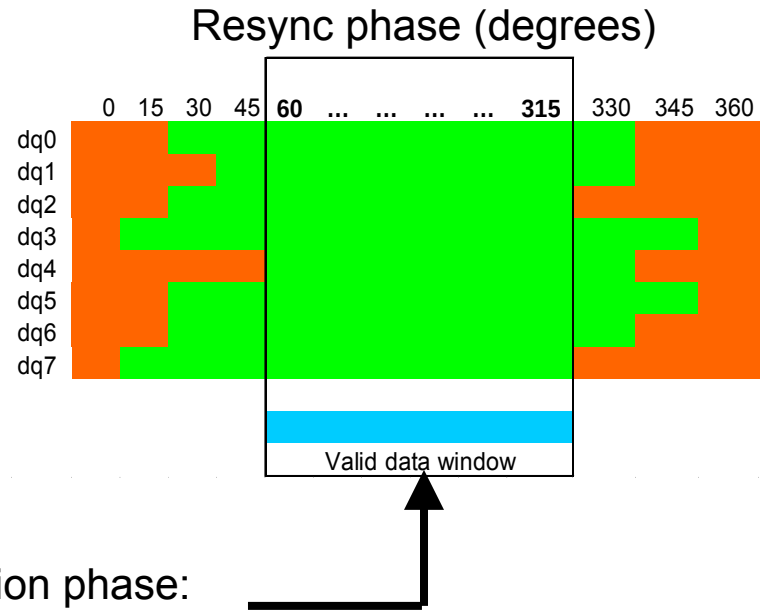
Timing margin based on dynamic calibration

Integrated System for Rapid Implementation



Calibration: Finding Best Resync Phase





Ideal resynchronization phase: maximum setup and hold margin

- Comparison done on a pin-by-pin basis
- Minimizes effects of process variations through accurate strobe placement

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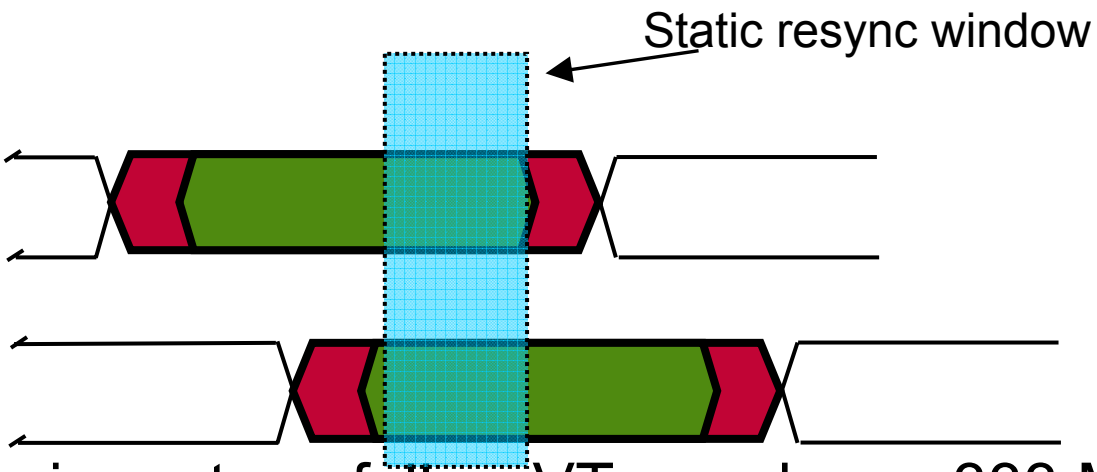
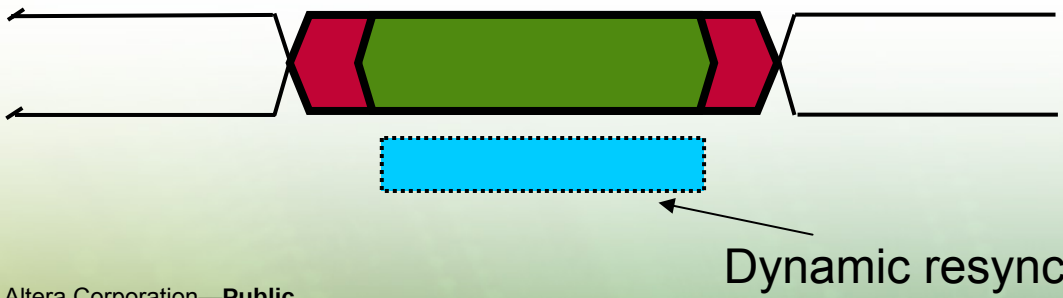
Static vs. Dynamic

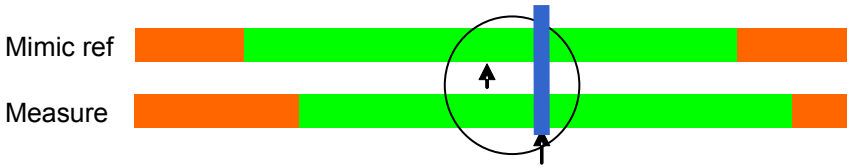
- Static timing analysis – good up to 267 MHz

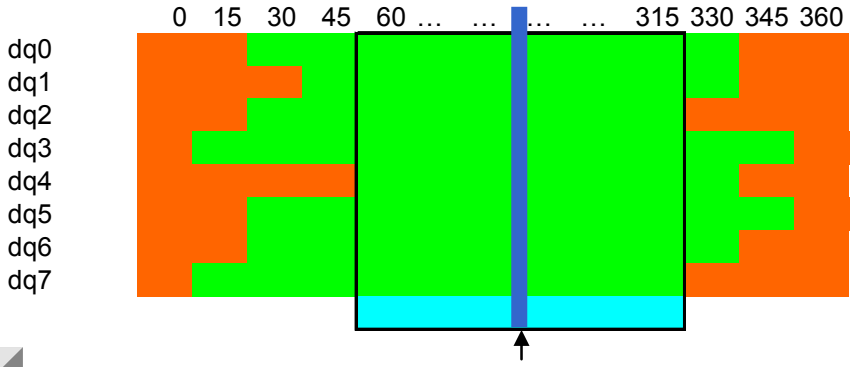


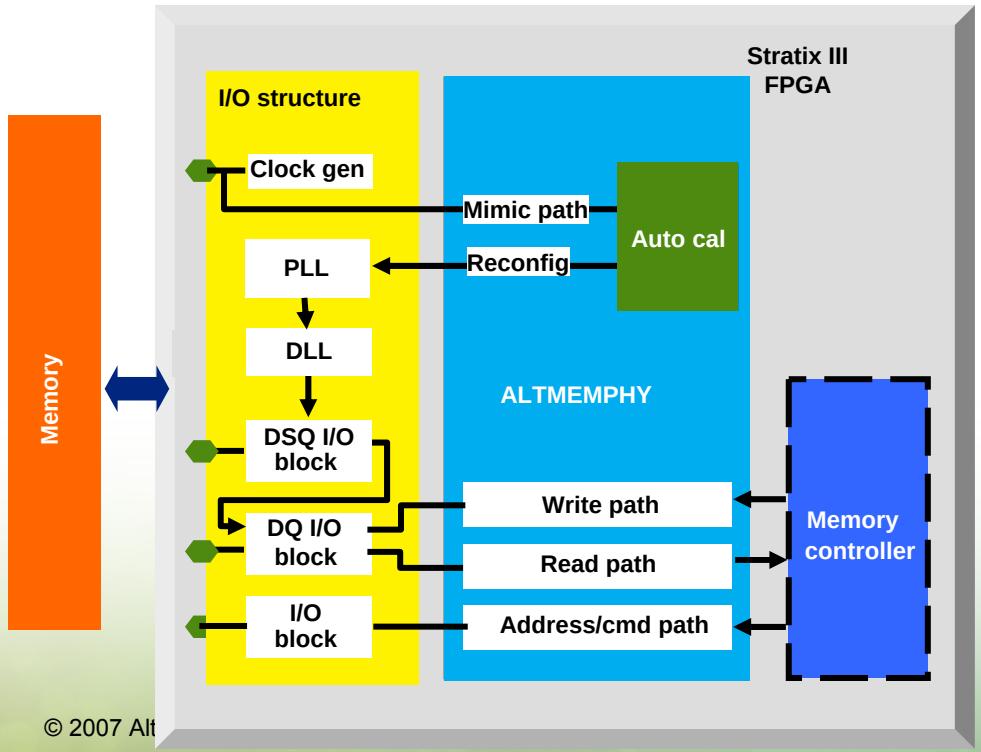
- Dynamic system, follow VT, good over 333 MHz



VT Tracking







- Maintain near-optimum resync clock phase as VT varies
- Continuous
- Transparent to user

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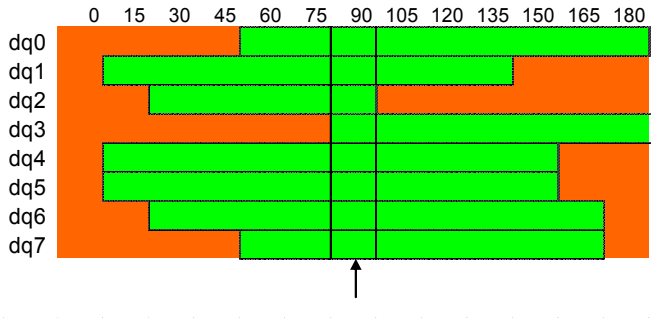
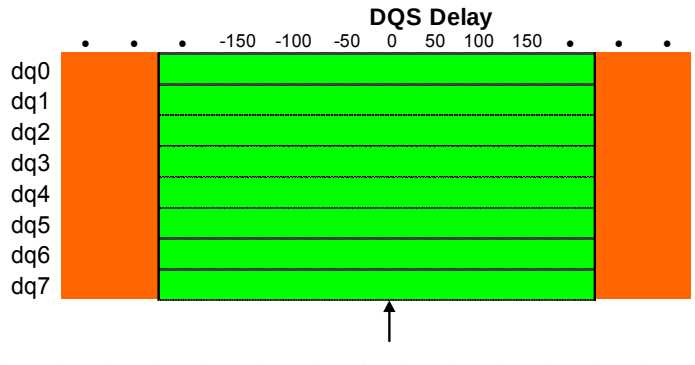
Skew Compensation

- Dynamic compensation (programmable delay chains) to deskew DQ data bus (memory, board, and controller skews)
- Increases capture margin at memory and FPGA/processor

Skew Compensation



Prior to deskew – small valid capture window



After deskew – maximize valid capture window

1. Write training pattern into external memory
2. Read back training data with different delay settings
3. Compare data and create pass/fail map
4. Select delays to maximize margin

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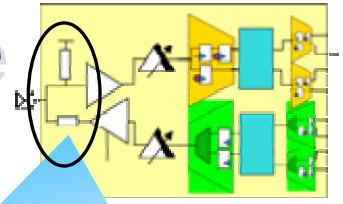
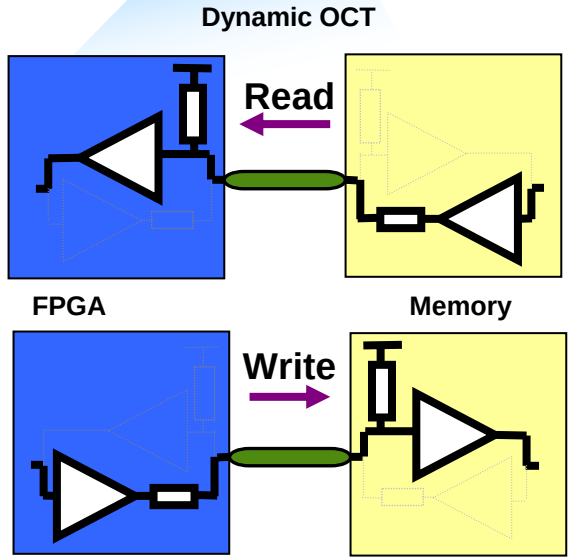
Calibrated Dynamic OCT For Proper Line Termination And Power Savings



- Mixed termination values in same bank
- Dynamically turned ON and OFF parallel termination – transparent operation
  - **Significant power saving**
    - 1.6 watts over 72-bit DDR2 bus
  - **Proper line termination** for bidirectional busses
  - **Reduce costs**
    - Ease routing congestion
    - Put the memories closer
    - Save external component cost

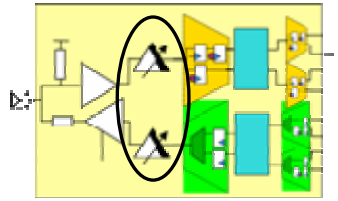


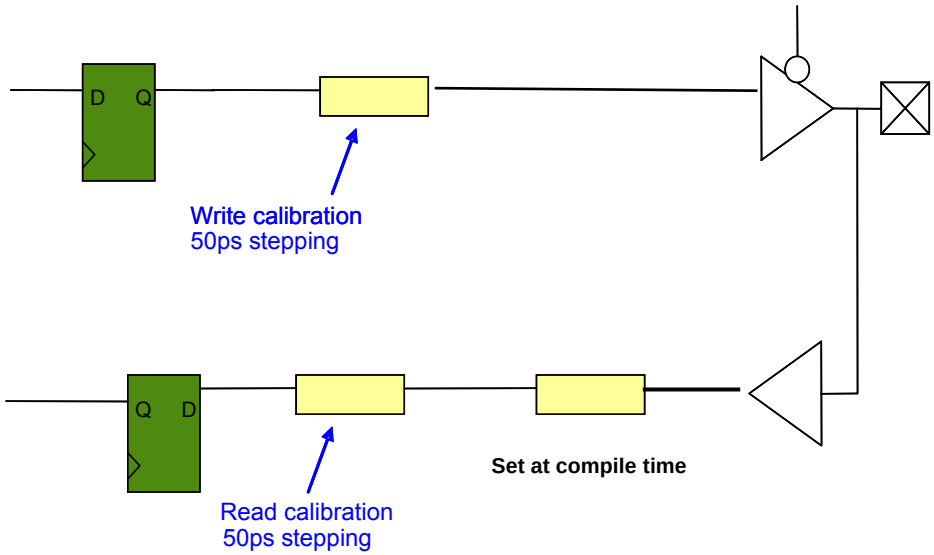
Single Ended Termination				
Function	Serial - Rs	Parallel - Rt	Dynamic	Calibratation
Value	25 / 50 default (20 to 60 Ω w/ Ext R)	50 Ω	Turn Rt off during writes	Rs & Rt
Comment	All banks +/- 5%	All banks +/- 5%	Saves power (Also off during bus idle)	PVT compensation (requires external resistor)

* Stratix III FPGA also supports on-chip differential termination (covered earlier)

** Final values and tolerances pending characterization

Variable Input and Output Delay For Deskew





Path	Run-time configurable	Step size	Set at compile	Step size	Output buffer	Step size	Total
Input	1100 ps	50 ps	2800 ps	400 ps			**3900 ps**
Output	1050 ps	50 ps			150 ps	50 ps	**1200 ps**

Resolution and absolute value pending characterization

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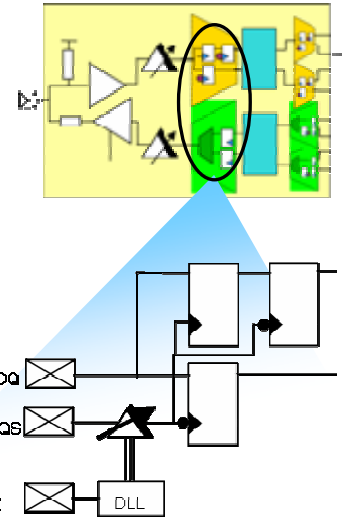
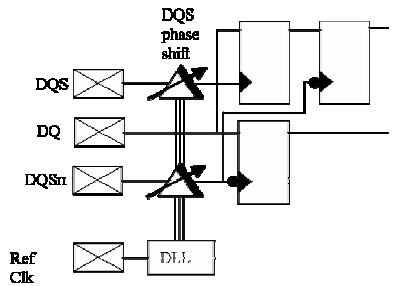
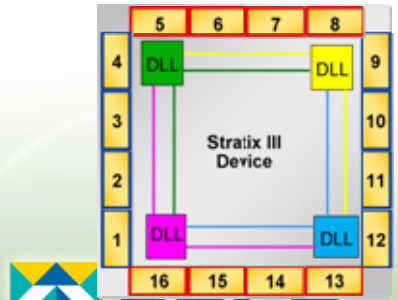
PVT-Compensated DQS Phase Shift

- DLL provides PVT compensation to DQS block
- DQS block phase shift incoming DQS
  - Non-intrusive to datapath
  - PVT compensated
  - Range of shifts of 0˚ to 180˚
  - Phase shift independent of DQ de-skew
- 4-, 8-, 9-, 16-, 18-, 32-, or 36-bit programmable DQ group widths
- Use DQS only, DQS/DQSn differential or DQS and DQSn separately (e.g., QDR II+)
- 4 DLLs support multiple independent memory interfaces
  - Each DLL has two outputs
  - Each I/O bank can access 2 DLLs
  - Allows multiple interfaces, separate frequencies

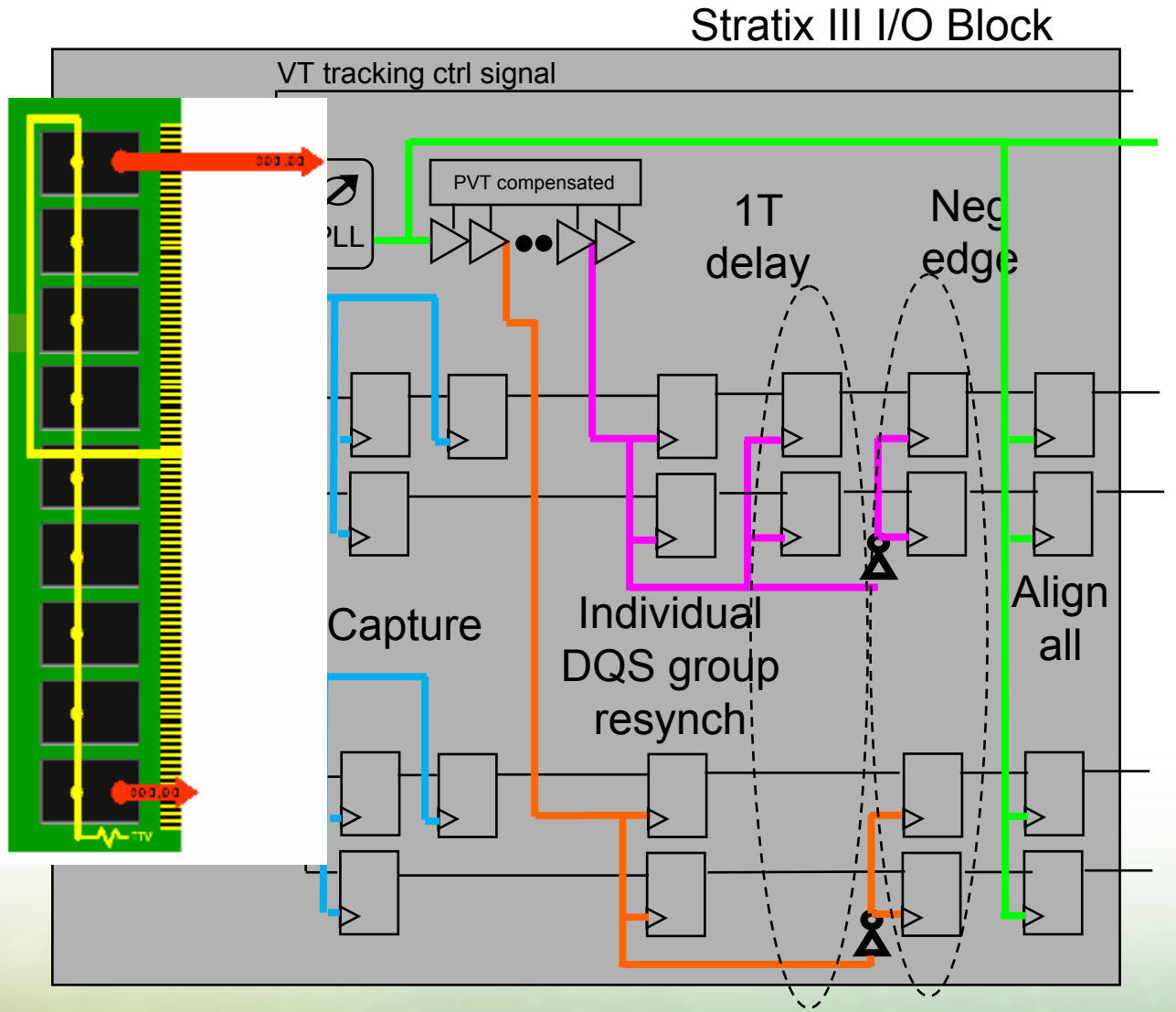


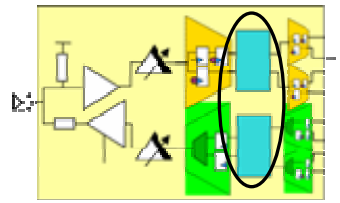


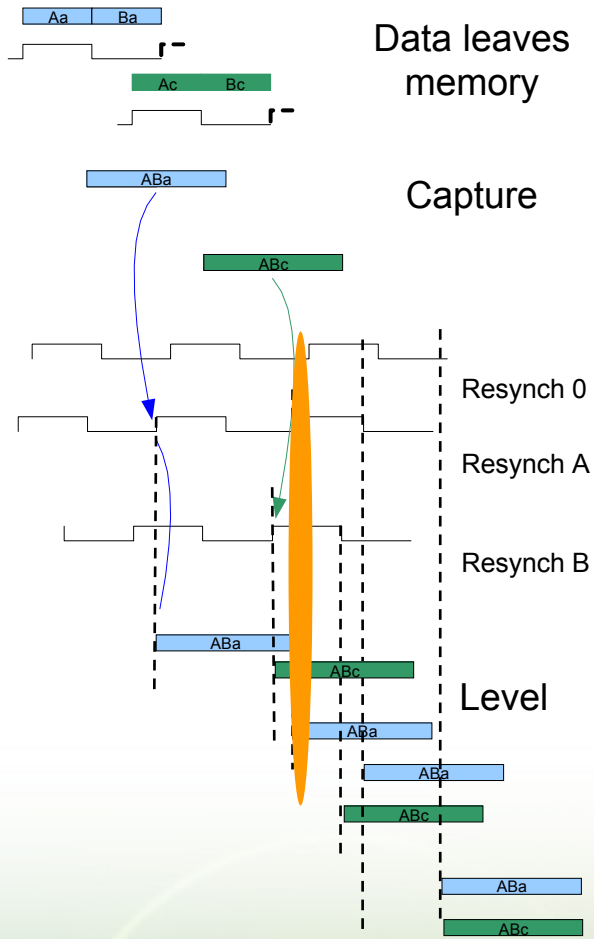


DDR3 Leveling in Stratix III FPGAs

Stratix III DDR3 Read Levelling







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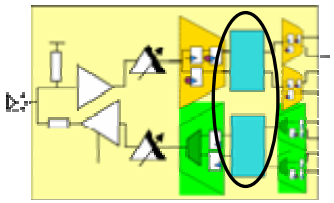
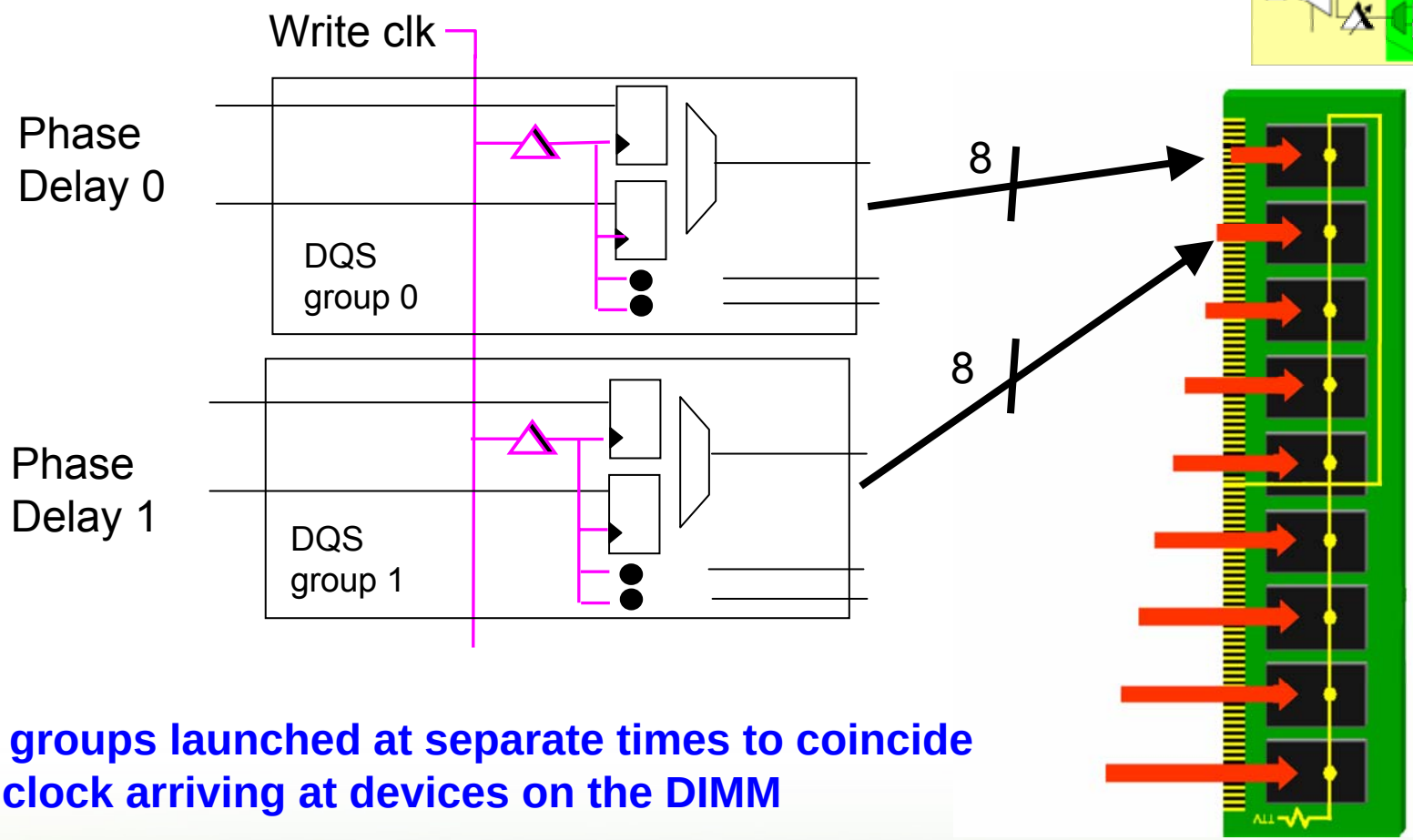
Write Leveling Built Into I/O For DDR3





DQS groups launched at separate times to coincide with clock arriving at devices on the DIMM

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DDR3 Features

	Stratix III FPGA	Virtex-5	Comment
Variable I/O delay			Required for inter DQS group DQ deskew
PVT-compensated individual DQS group delay			Required for read and write leveling
1T delay registers			Required for read and write leveling
Neg edge registers			Required for read and write leveling
All contained directly in I/O			Reduces clock resources consumed, allows higher frequency of operation, saves cost of external components

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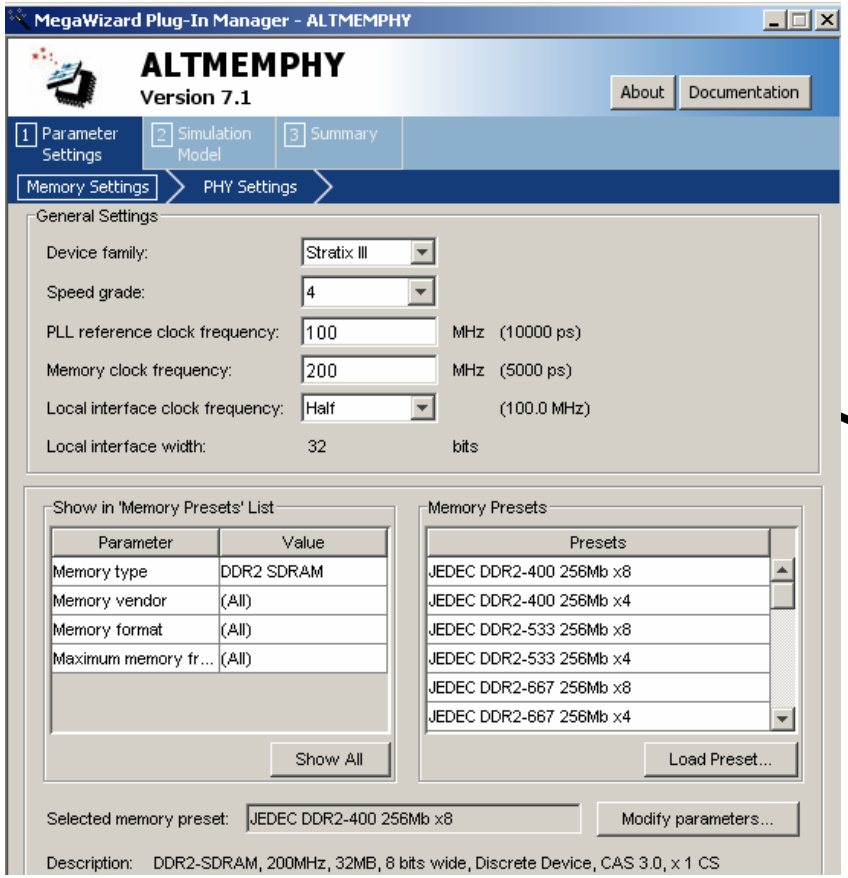
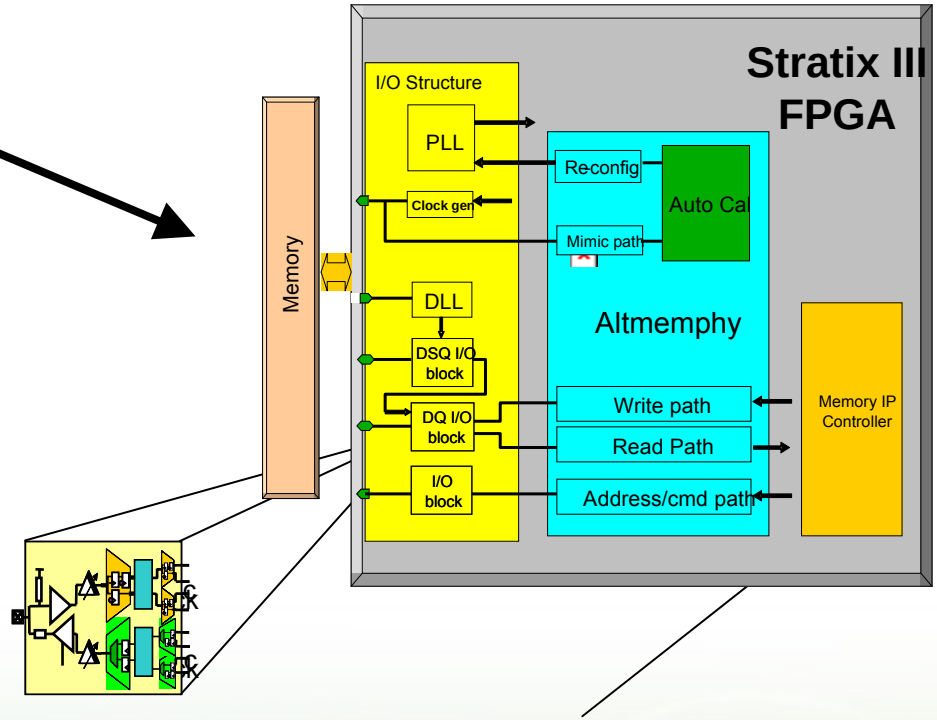
Software Tools

Adding the IP: GUI Tool For Rapid Integration



- Altmemphy integrates PLL, DLL, DQS, and DQ hard macros



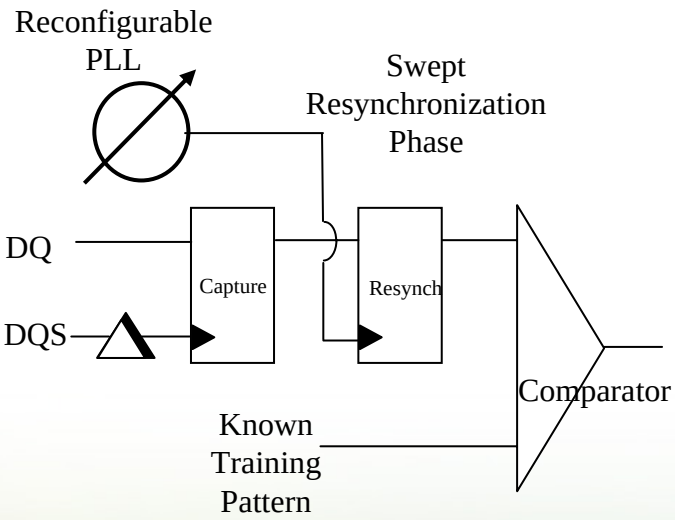
- Constrained with SDC
  - Synopsys Design Constraints (SDC)
  - Industry standard
  - Easy to constrain data with respect to source synchronous clock

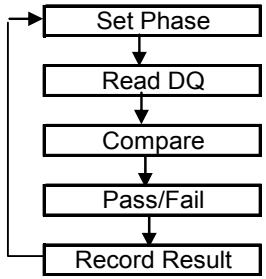
Altera or user-defined controller

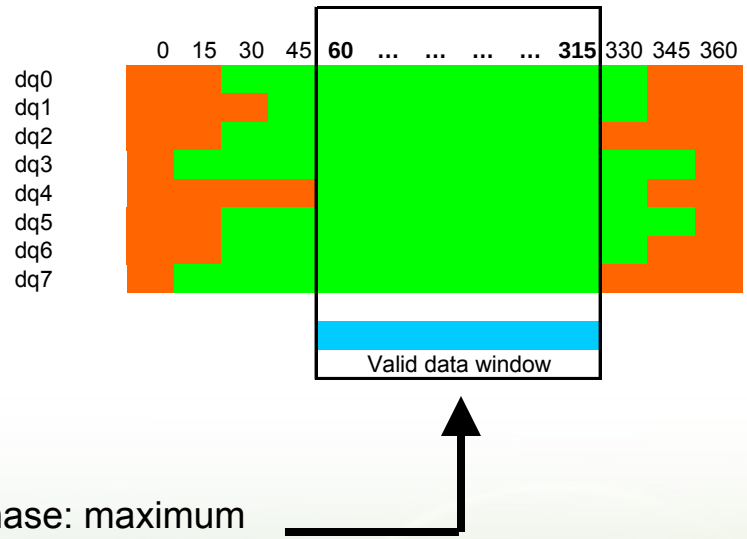
CY8 For graphic on right, need a noun after Stratix III per Altera trademark rules....You can have it say: Stratix III FPGA. (I can't edit this graphic)
Christine Young, 2007-8-24

Altmemphy IP Calibration at Start-up

- Calibration – Removes process variation from FPGA and memory
  - Sweep all resynch phases for all DQ pins
  - Build map: pin-by-pin basis
  - Select best resynch phase



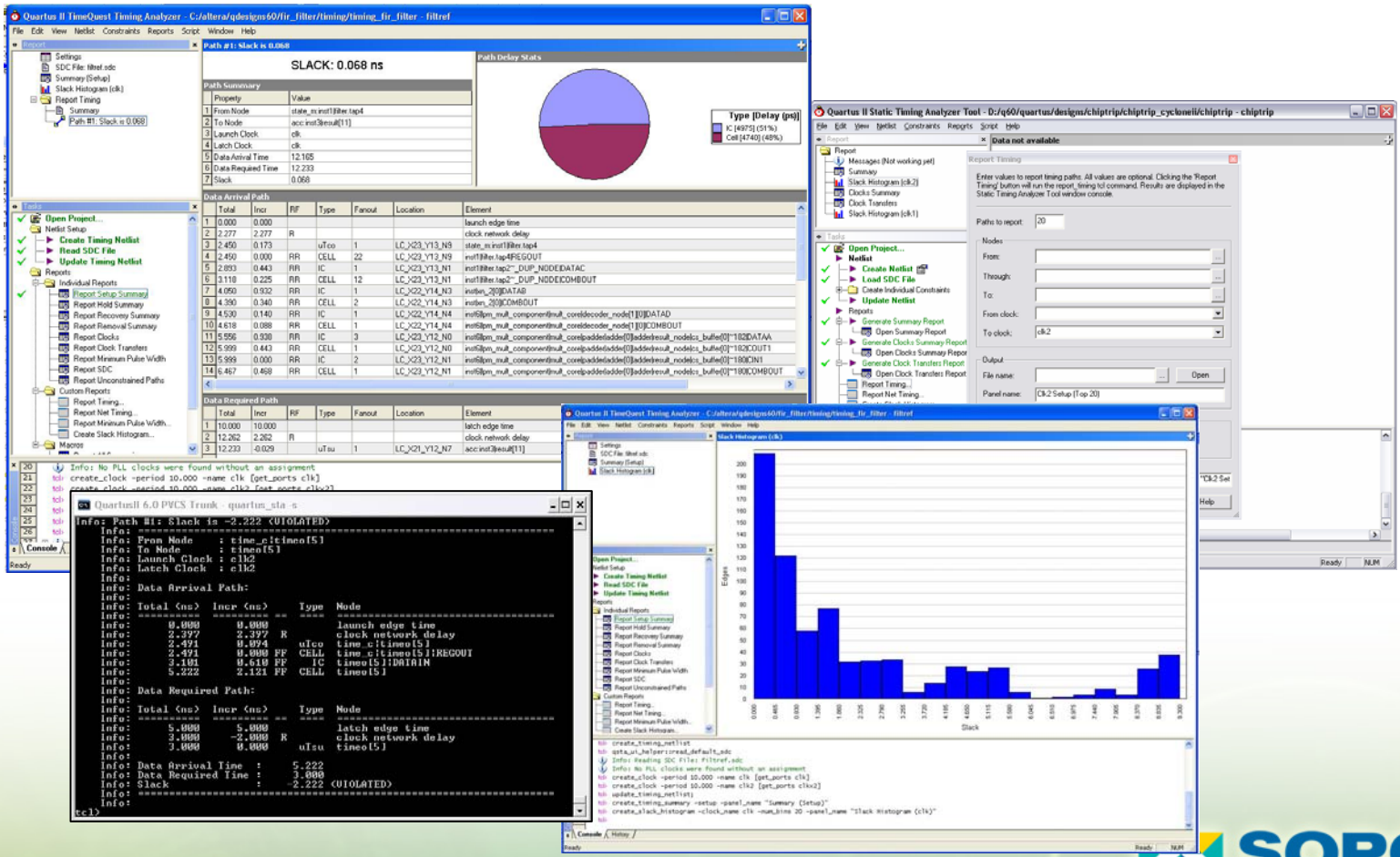




Ideal resynch phase: maximum setup and hold margin

Closing Timing On Source-Synchronous Interface With TimeQuest

- ASIC-strength timing analysis tool



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Read Timing Analysis – DDR3-800

Parameter	Timing without calibration (ps)*	Timing with calibration (ps)*	Description
Period	2,500	2,500	400 MHz
t_{HP}	1,250	1,250	Ideal half period time
DRAM uncertainties	500	200	DQ-DQ and DQS-DQ skew reduced via deskew
T_{DCD}	125	125	FPGA output clock duty cycle distortion (±5%)
FPGA + board uncertainties	550	300	Uncertainties include DLL jitter, setup and hold, clock tree skew, SSI jitter
Margin	75	625	Read timing margin

Write Timing Analysis – DDR3-800

Parameter	Timing without calibration (ps)*	Timing with calibration (ps)*	Description
t_{HP}	1,250	1,250	Ideal half period time
DRAM uncertainties	425	200	DQ-DQ and DQS-DQ skew reduced via deskew
T_{DCD}	125	125	FPGA output clock duty cycle distortion (±5%)
FPGA + board uncertainties	575	300	Uncertainties include PLL jitter, clock network skew, PRBS data pattern jitter, rise/fall mismatch, and SSO pushout
Margin	125	625	Write timing margin

Performance Summary

- Performance shown for 1.1V core
- Frequency of operation is **expected to go up** post characterization

Memory standards	I/O standards	-2 speed grade (MHz)		-3 speed grade (MHz)		-4 speed grade (MHz)		Maximum data rate
		Column I/Os	Row I/Os	Column I/Os	Row I/Os	Column I/Os	Row I/Os	Fastest speed
DDR SDRAM	SSTL-2	200	200	200	200	200	200	400 Mbps
DDR2 SDRAM	SSTL-1.8	400	300	333	267	333	267	800 Mbps
DDR3 SDRAM	SSTL-1.5	400	300	333	TBD	333	TBD	800 Mbps
RLDRAM II	1.8V HSTL	400	300	300	250	300	250	800/1,600 Mbps
QDR II SRAM	1.8V and 1.5V HSTL	350	300	300	250	300	250	1,400 Mbps
QDR II + SRAM	1.8V and 1.5V HSTL	350	300	300	250	300	250	1,400 Mbps

The Only FPGA with DDR3 Support

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Conclusion

- Stratix III FPGAs offer the highest reliable frequency of operation across PVT
  - DQ/DQS block
  - Dynamic calibration with PVT compensation
  - Deskew feature
- Stratix III FPGAs are the only FPGAs to offer DDR3 memory interface support
  - Includes support for DDR3 DIMMs

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Thank You!