

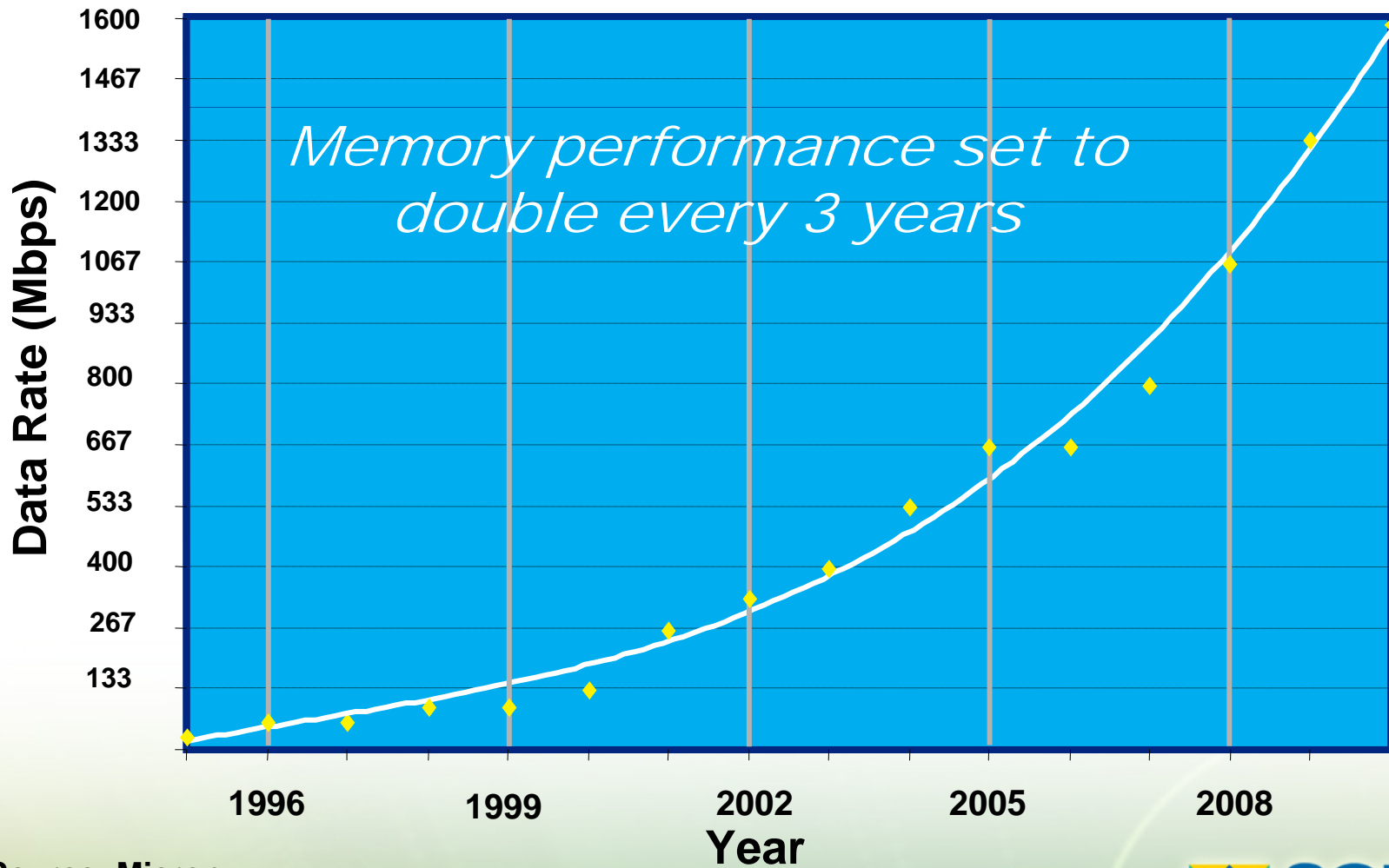


Designing Next-Generation DDR3-based Memory Interfaces

Agenda

- DDR3 timing margin challenges
- DDR3 features in Stratix[®] III FPGAs
- DDR3 smart interface module
- Timing closure tools
- Summary

Mainstream Memory Trends



Source: Micron

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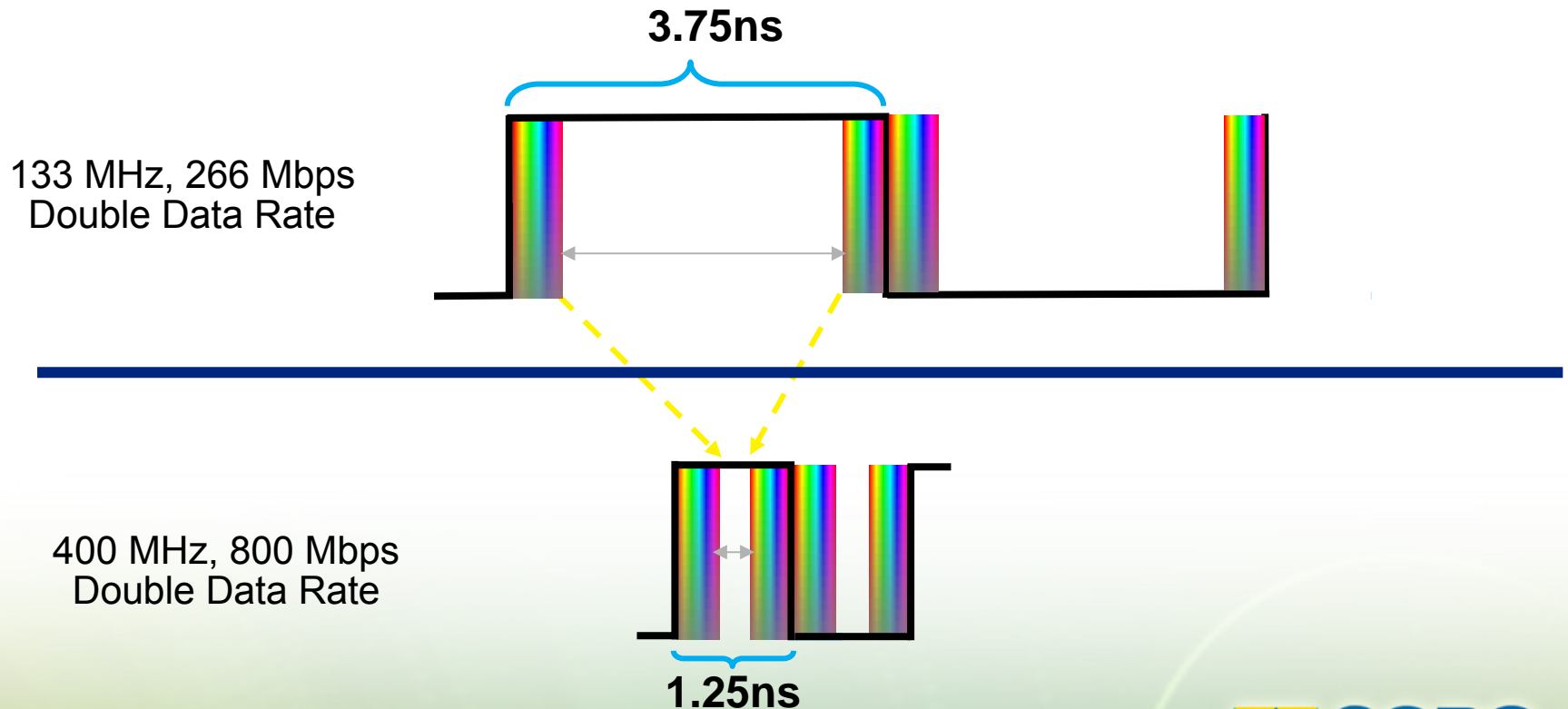


DDR3 SDRAM Advantages

- Lower system power
 - DDR3 power: 30% to 40% lower than DDR2
 - FPGA Programmable Power Technology
- Higher density memories
 - Same board area
- Lower price over system lifetime
 - DDR3 price cross-over projected 2 years out
- Dynamic On-Chip Termination (OCT)
 - Proper line terminations and lower costs

Timing Margin Challenges

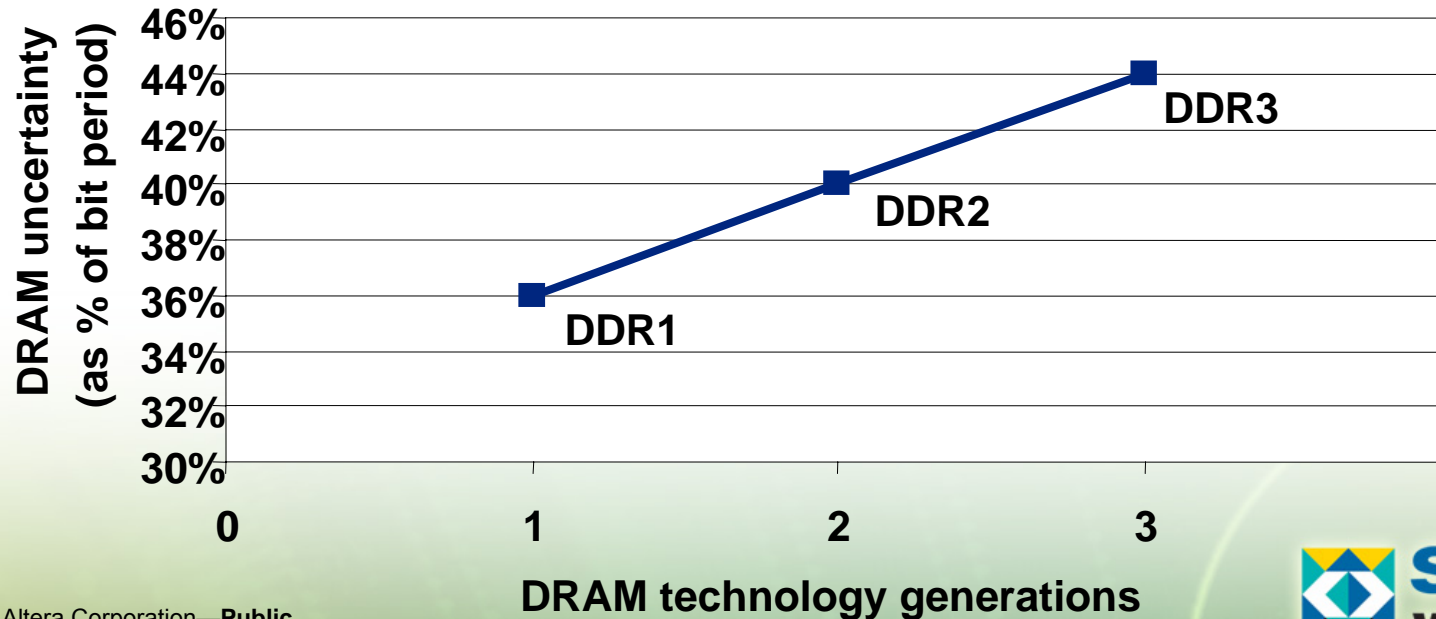
- Memory and board uncertainties do not scale with frequency
- Effects designers could previously ignore are now significant proportions of the cycle



Memory Uncertainty Increasing..

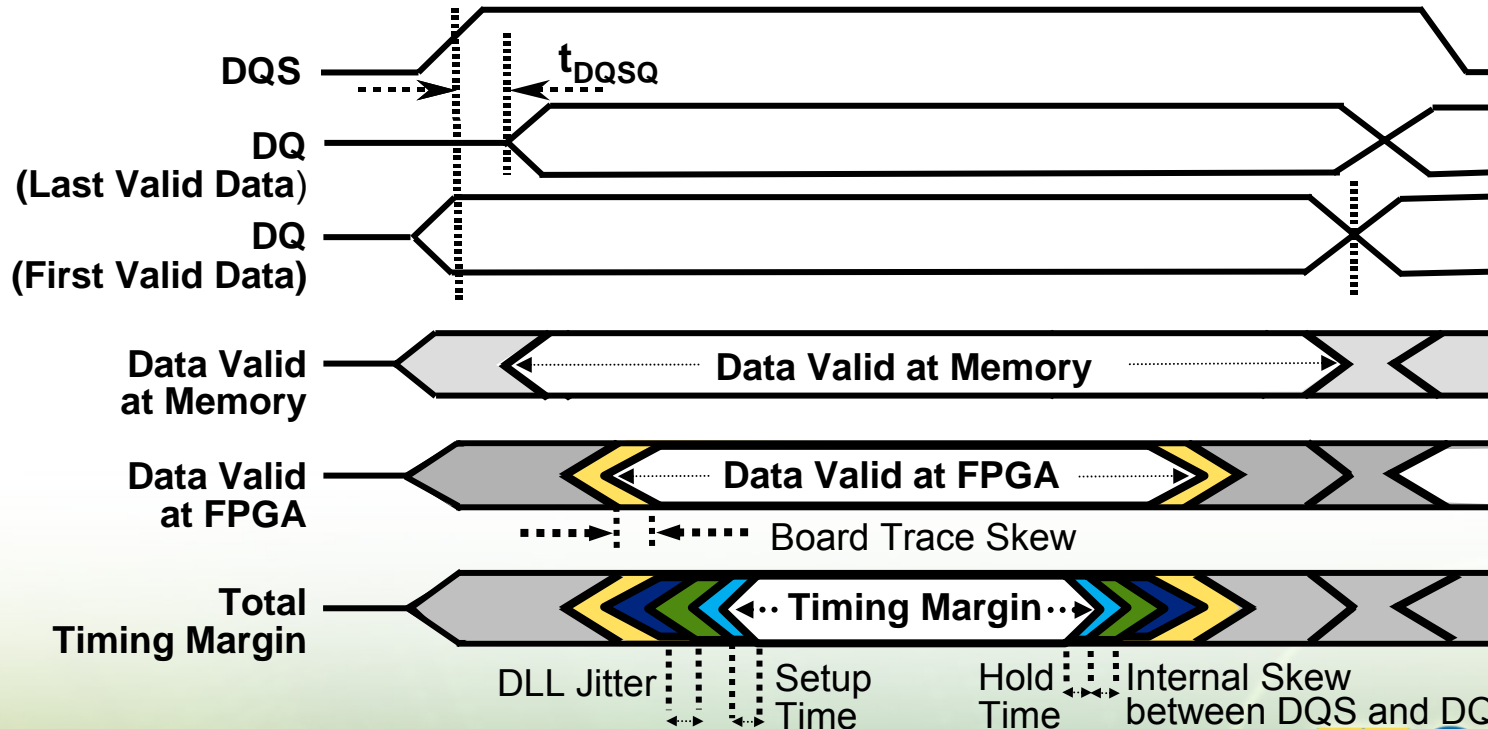
Memory parameters (ps)	DDR-400	DDR2-800	DDR3-800
t_{CK} clock period	5,000	2,500	2,500
Bit time	2,500	1,250	1,250
t_{DQSQ} DQS to DQ skew	400	200	200
t_{QH} data output hold time from DQS	2,000	950	900
Data eye at DRAM	1,600	750	700
% bit period	64%	60%	56%
DRAM uncertainties	36%	40%	44%

Source: Jedec



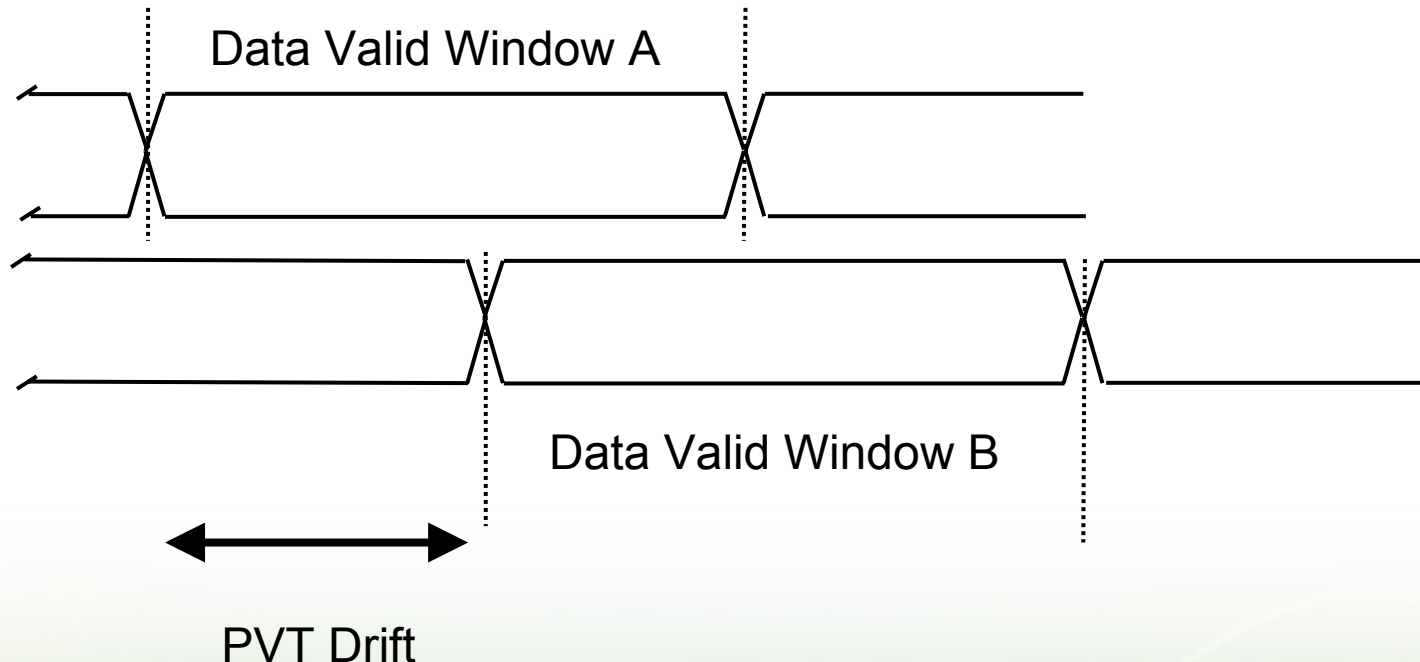
Shrinking Data Valid Window

- Following effects reduce the data valid window
 - The skew between first data valid and last data valid
 - Board trace skew
 - DLL jitter for DQS phase shift circuitry
 - Internal skew between DQS and DQ
 - Setup and hold time



Moving Data Valid Window

- Data valid window shifts with process, voltage, and temperature (PVT) variations





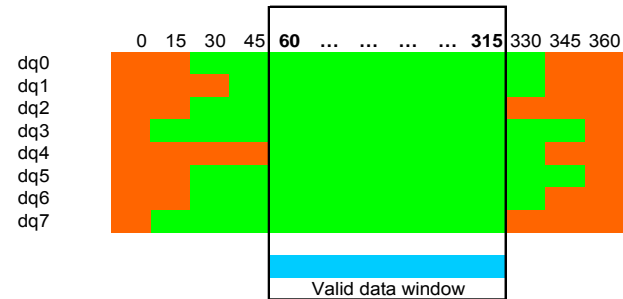
So how to tackle these challenges?

Some Techniques

Dynamic Calibration

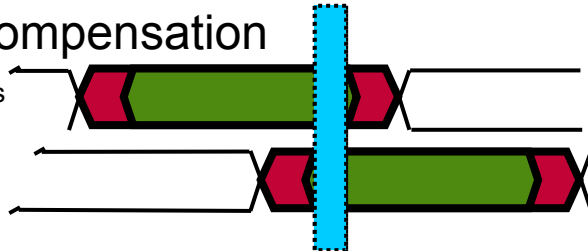
Without calibration: complex static timing analysis, narrow data valid window

With calibration: accurate strobe placement, wider data valid window

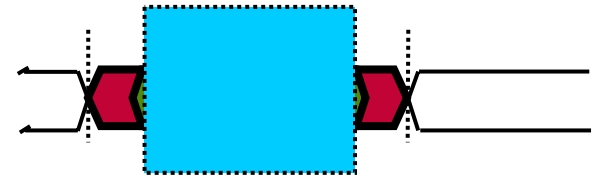


VT Compensation

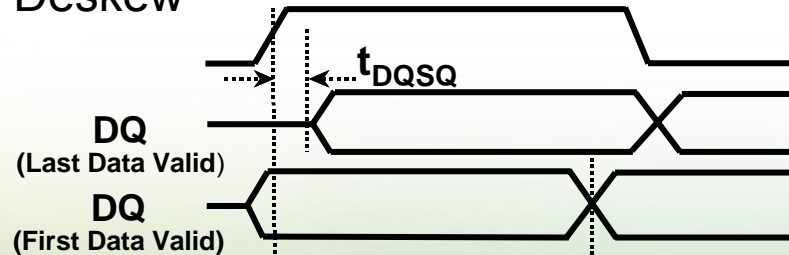
Data shifts due to VT variations



Voltage and temperature tracking

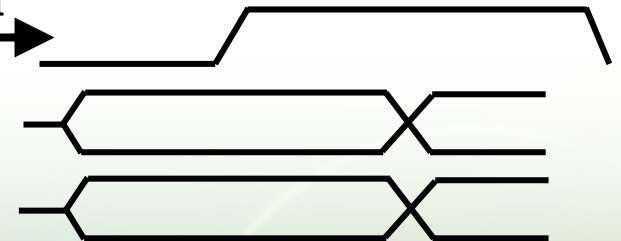


Deskew



DQS phase shift

Deskew





Leveling in DDR3 Interfaces

DDR3 Read-Write Leveling

■ Leveling

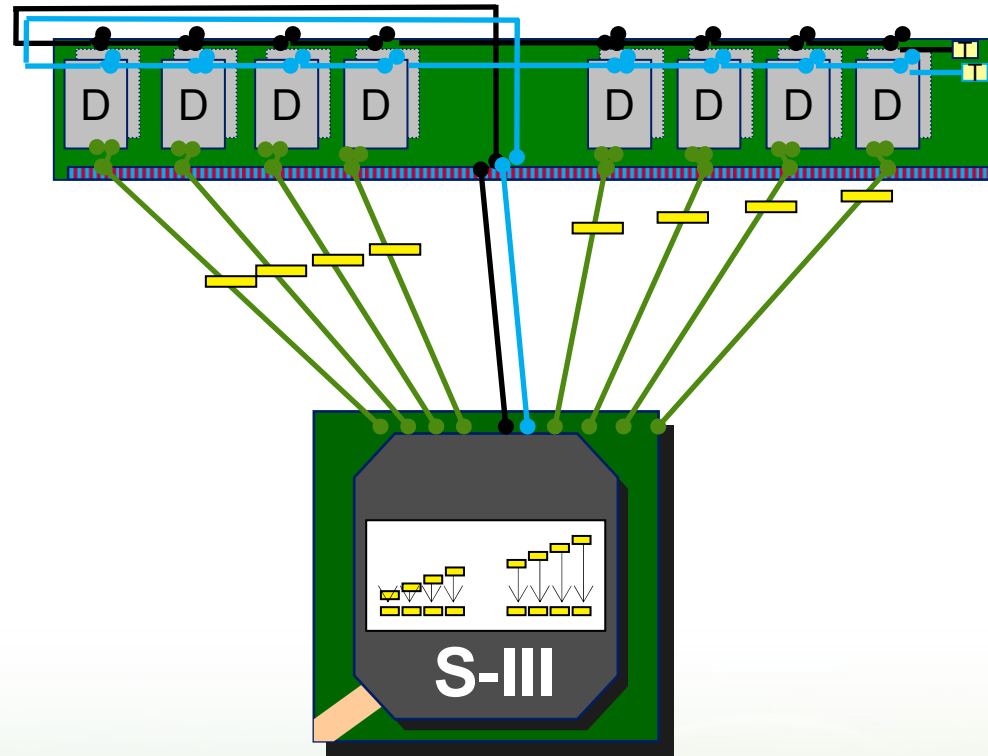
- Required to compensate for DDR3 (Jedec) fly-by topology which causes flight time skew between CA/clock and DQS across a DIMM

■ Write leveling

- For writes, t_{DQSS} at DRAM needs to be kept at $\pm 0.25 t_{CK}$

■ Read leveling

- Read data arrival time at memory controller could be spread over 2 clk cycles

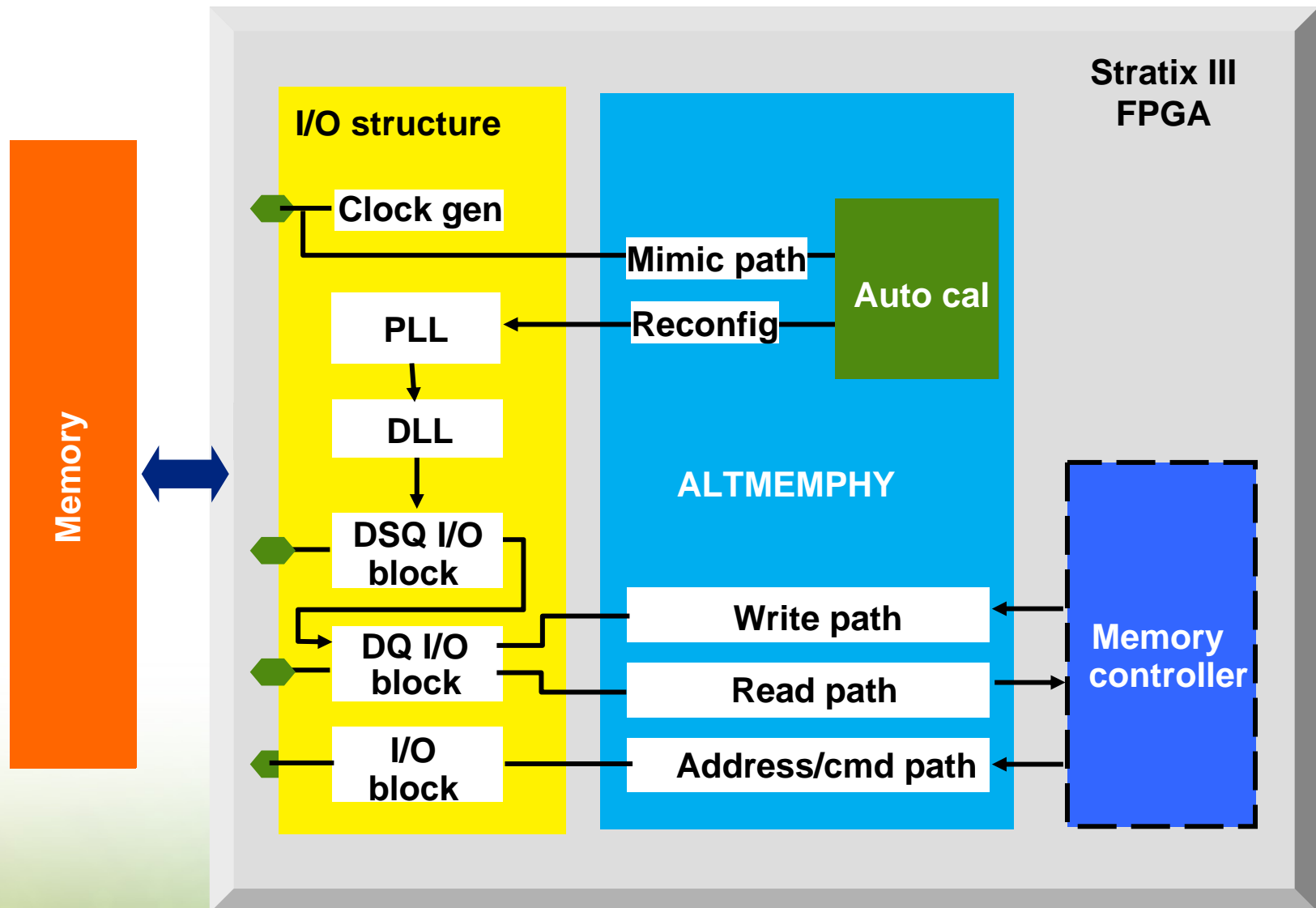


Courtesy: Qimonda



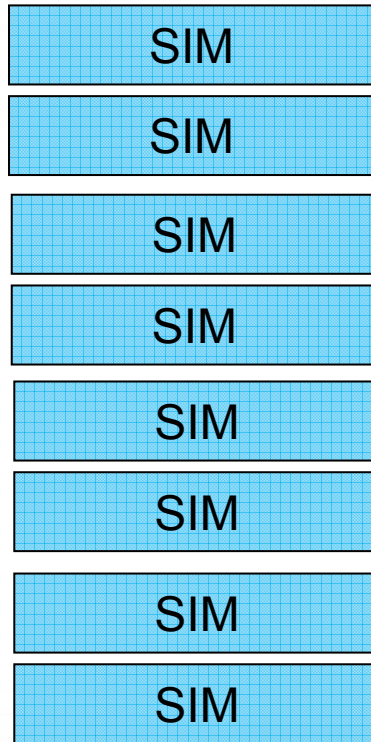
DDR3 Features in Stratix III FPGAs

DDR3 Smart Interface Module Using Stratix III FPGAs

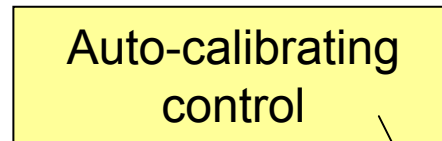


Smart Interface Module

Smart Interface Module



+



=

**Intelligent
Memory
Interface**

Algorithm to control silicon
and buy-back margin

Silicon features to recover margin
and enable high-frequency
operation

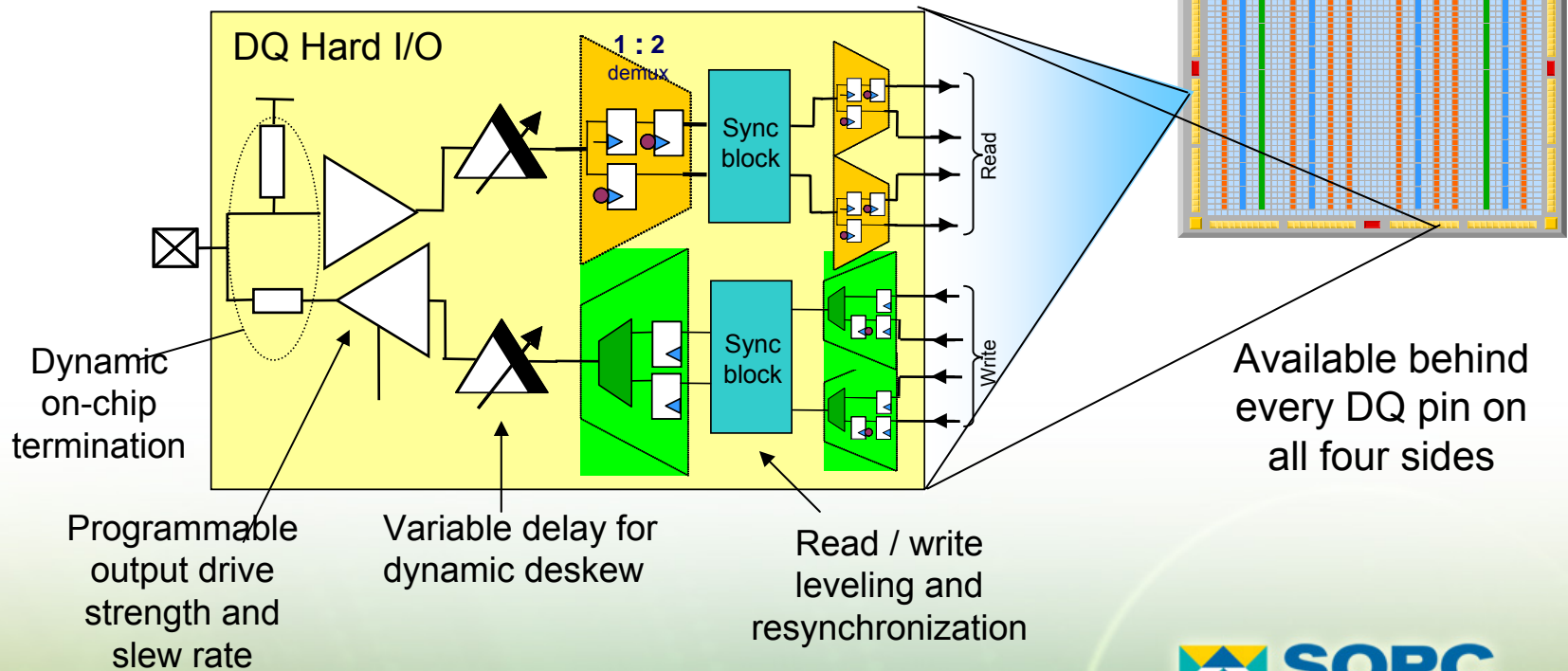
**Provides highest
reliable frequency of
operation across**

PVT



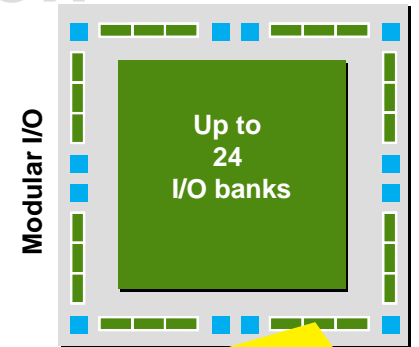
Stratix III DDR I/O Block

- Programmable I/O delay for deskew
- Controllable drive strength and slew rate for best-in-class signal integrity (SI)
- Half data rate option for design simplification
- Read / write leveling for DDR3 performance
- 31 embedded registers
 - Manage clock domain crossing and rate changing directly in I/O



Electricals And Vertical Migration

- Support over 40 I/O standards
- Mixed termination values in same bank
- New modular bank structure eases vertical migration
 - E.g. F1152 package identical for all family members over 8 die sizes



24- to 48-bit banks with common structure

	Device	9 Deep		8 Deep		
		484-Pin	780-Pin	1152-Pin	1517-Pin	1760-Pin
		FBGA	FBGA	FBGA	FBGA	FBGA
		1.0 mm	1.0 mm	1.0 mm	1.0 mm	1.0 mm
		23 x 23	29 x 29	35 x 35	40 x 40	43 x 43
Stratix III Logic	EP3SL50	288	432	672	1008	1344
	EP3SL70	288	432	672	1008	1344
	EP3SL110	288	432	672	1008	1344
	EP3SL150	288	432	672	1008	1344
	EP3SL200	288	432	672	1008	1344
	EP3SE260	288	432	672	1008	1344
	EP3SL340	288	432	672	1008	1344
Stratix III Enhanced	EP3SE50	288	432	672	1008	1344
	EP3SE80	288	432	672	1008	1344
	EP3SE110	288	432	672	1008	1344
	EP3SE260	288	432	672	1008	1344

Competitive FPGAs force you to re-spin board to get more logic

Differential I/O
Differential HSTL
Differential SSTL
Single-ended I/O
SSTL2, 18, 15 Class I and II
HSTL 18, 15, 12 Class I and II



Pin Capacitance

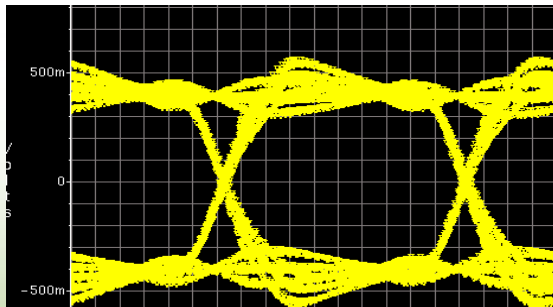
■ Basic physics, pin capacitance matters

- Higher capacitive loading = lower performance
 - Assume $R = 50$ ohm trace impedance

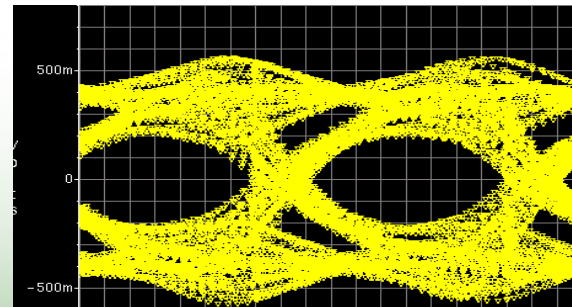
	Stratix III FPGA	Stratix II FPGA	Virtex 5 FPGA	Virtex 4 FPGA
Vertical I/O pin capacitance	5 pf	5 pf	9 pF	12 pF
Low pass filter - 3dB point	637 MHz	637 MHz	353 MHz	265 MHz

- Skew and jitter uncertainties will reduce this number further
 - However, low pin cap and high toggle rates are mandatory for high performance

■ Affect of pin capacitance in action



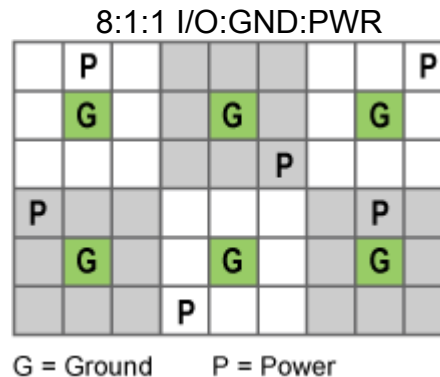
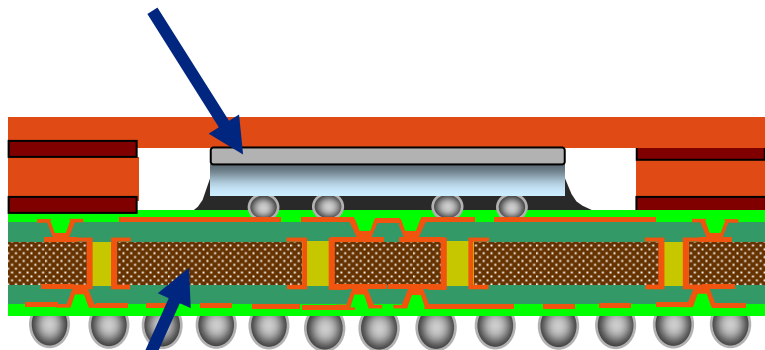
Stratix II FPGA



Stratix II FPGA with x2 pin cap
deliberately added

Die, Package, and Digital SI Enhancements

Significant silicon features	Benefits
<ul style="list-style-type: none"> Adjustable slew rate control (4 settings) Advanced on-chip termination User staggered output delay control On-die capacitors 	<ul style="list-style-type: none"> Reduce $\partial i/\partial t$ Proper termination Reduces simultaneous switching noise (SSN) Improve power distribution network (PDN) quality



In practise closer to 7:1:1

Significant package features	Benefits
<ul style="list-style-type: none"> On-package decoupling capacitors 8:1:1 – I/O:GND:PWR ratio –Max distance between I/O and gnd = 1 	<ul style="list-style-type: none"> Reduces loop inductance → reduces SSN Improve PDN quality





Calibration and Tracking

Dynamic Calibration

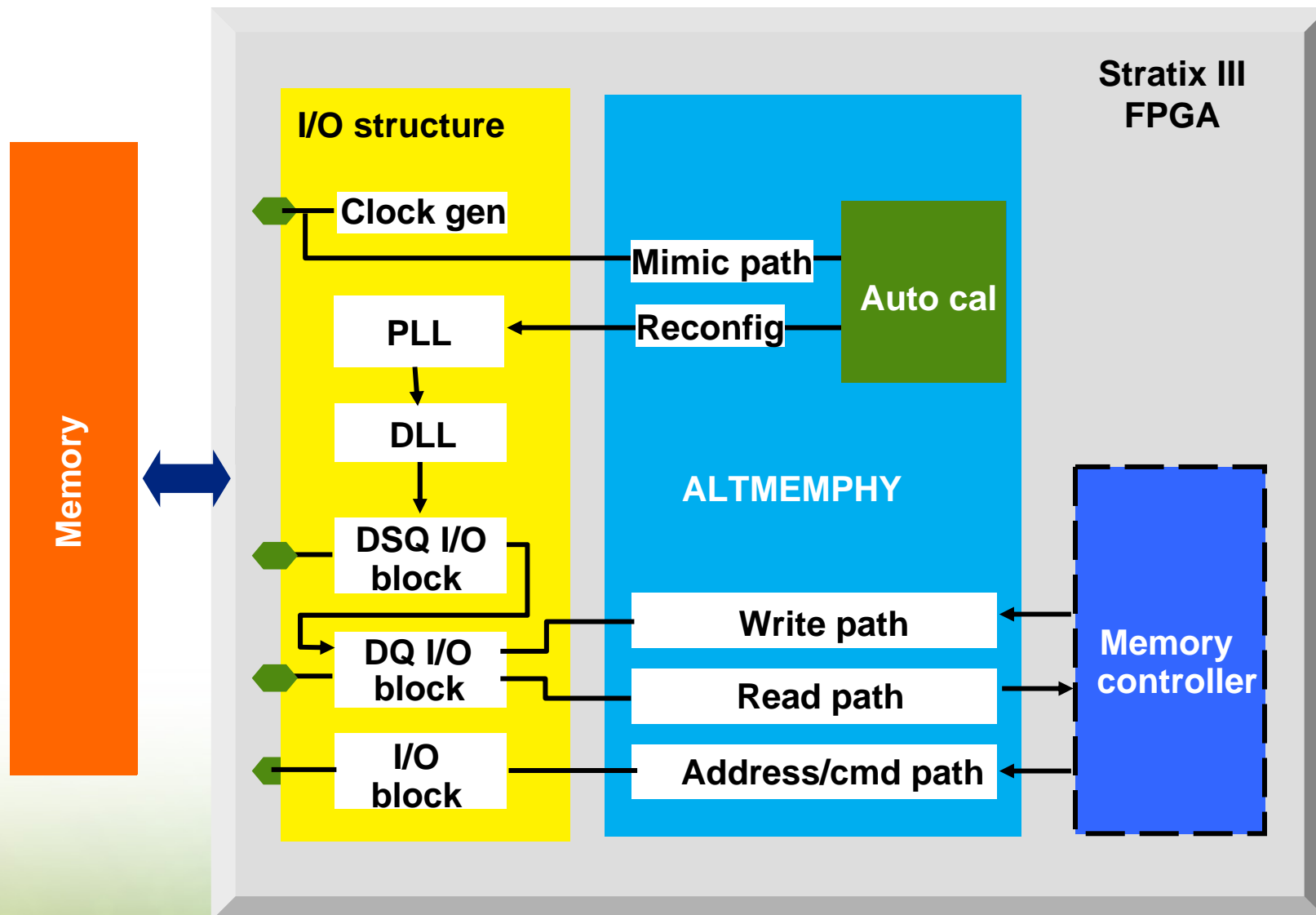
Timing margin based on static timing analysis



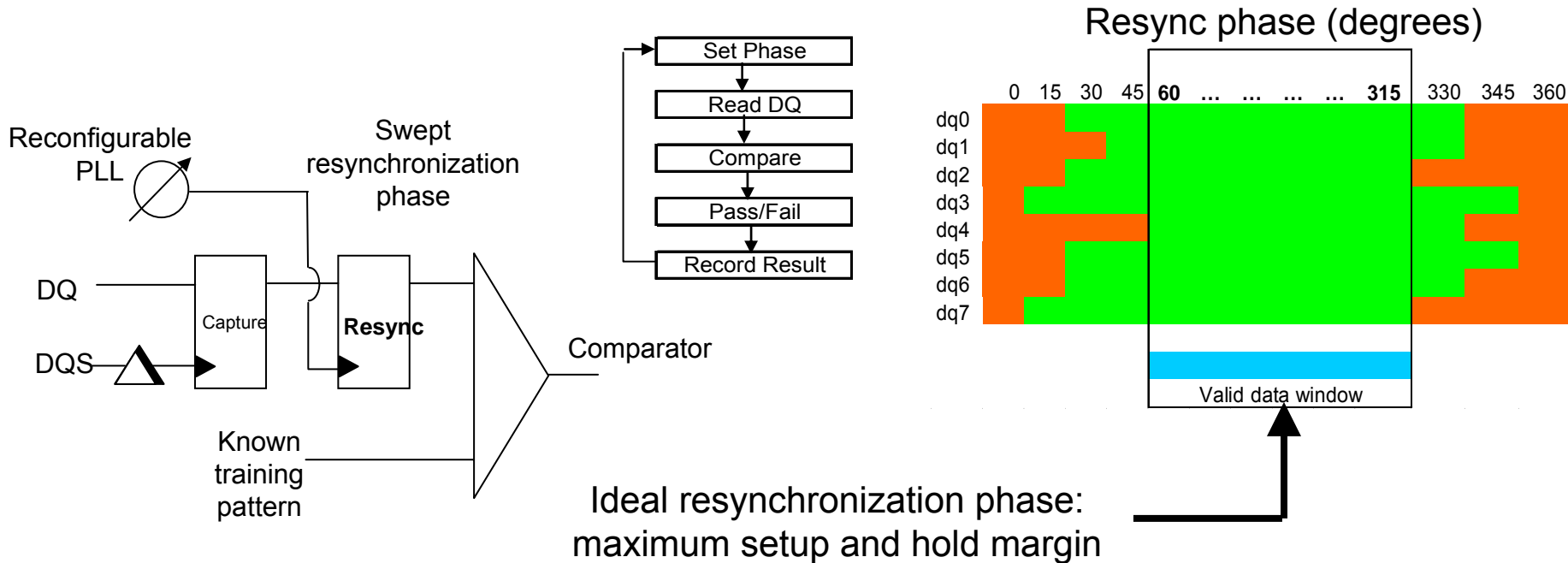
Timing margin based on dynamic calibration



Integrated System for Rapid Implementation



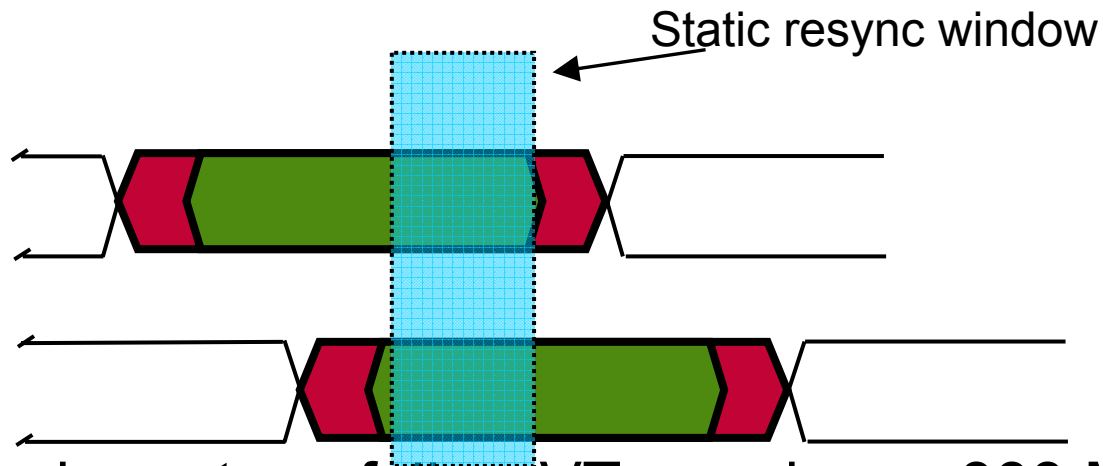
Calibration: Finding Best Resync Phase



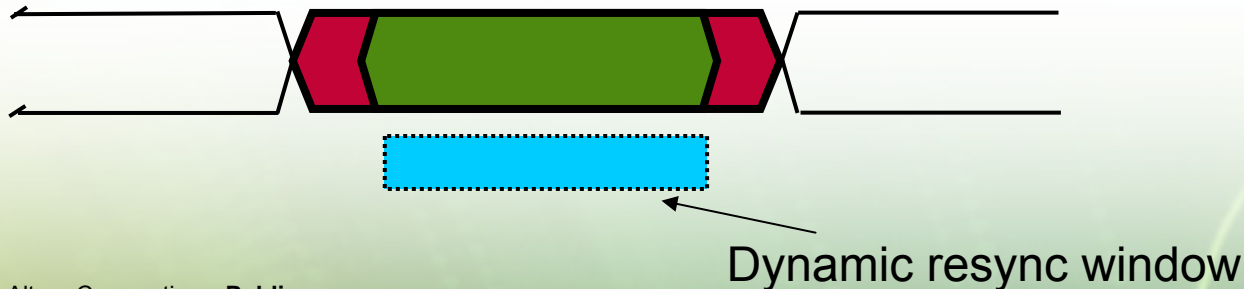
- Comparison done on a pin-by-pin basis
- Minimizes effects of process variations through accurate strobe placement

Static vs. Dynamic

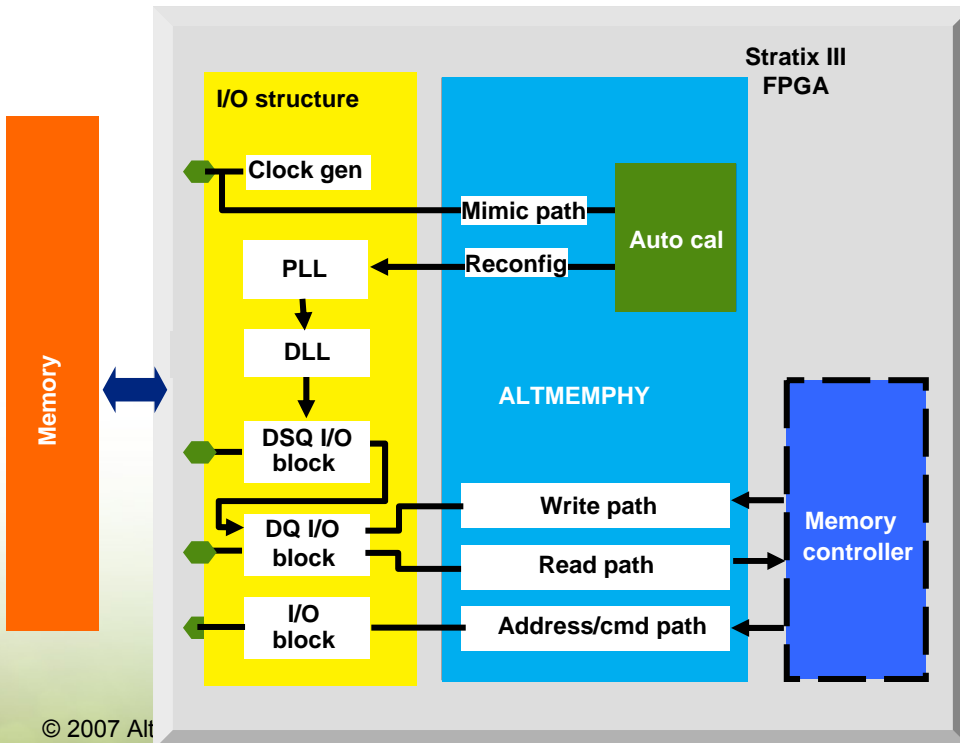
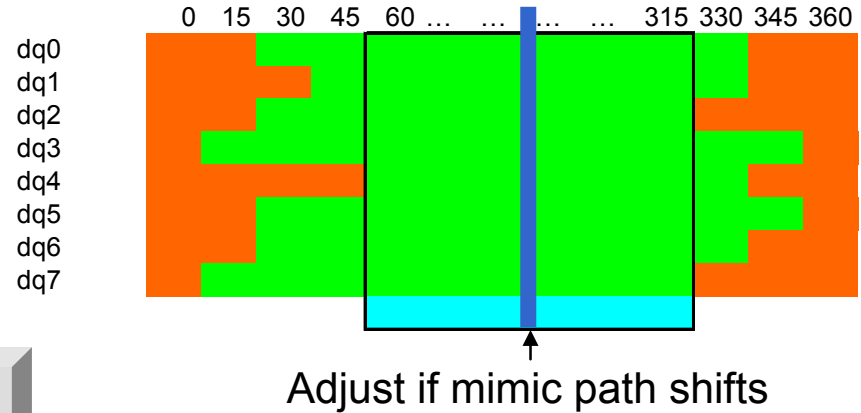
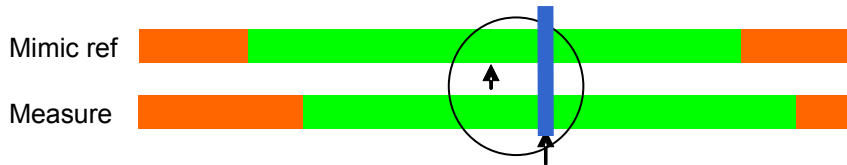
- Static timing analysis – good up to 267 MHz



- Dynamic system, follow VT, good over 333 MHz



VT Tracking



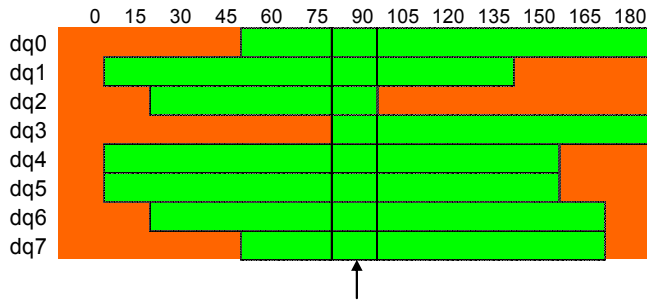
- Maintain near-optimum resync clock phase as VT varies
- Continuous
- Transparent to user

Skew Compensation

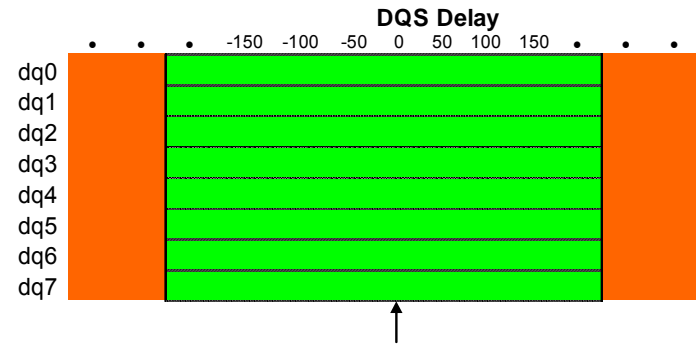


- Dynamic compensation (programmable delay chains) to deskew DQ data bus (memory, board, and controller skews)
- Increases capture margin at memory and FPGA/processor

Skew Compensation



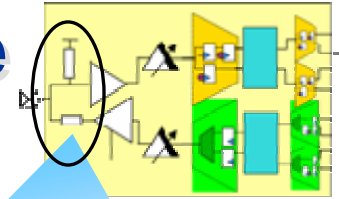
Prior to deskew – small valid capture window



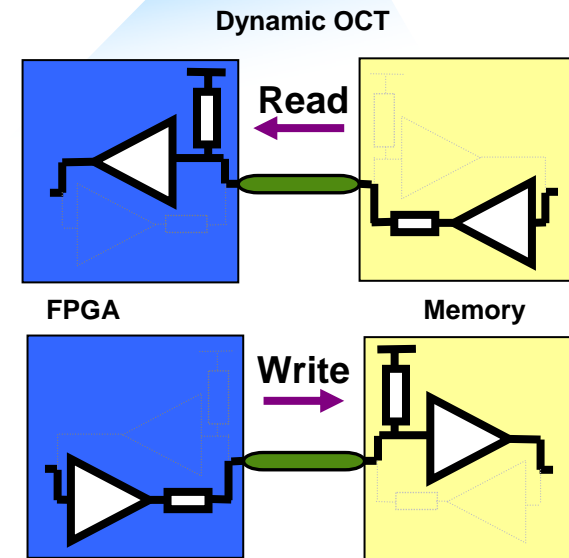
After deskew – maximize valid capture window

1. Write training pattern into external memory
2. Read back training data with different delay settings
3. Compare data and create pass/fail map
4. Select delays to maximize margin

Calibrated Dynamic OCT For Proper Line Termination And Power Savings



- Mixed termination values in same bank
- Dynamically turned ON and OFF parallel termination – transparent operation
 - **Significant power saving**
 - 1.6 watts over 72-bit DDR2 bus
 - **Proper line termination** for bidirectional busses
 - **Reduce costs**
 - Ease routing congestion
 - Put the memories closer
 - Save external component cost

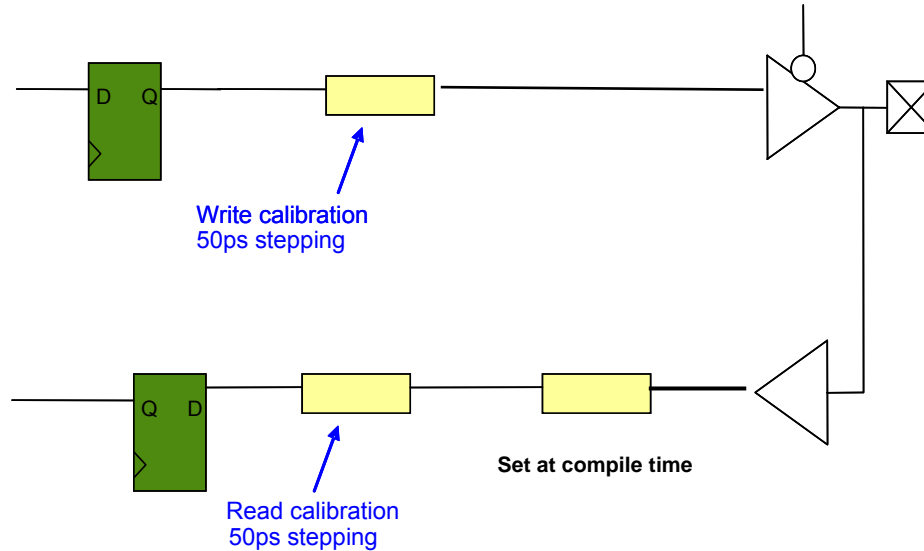
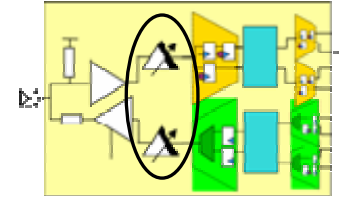


Single Ended Termination				
Function	Serial - R_s	Parallel - R_t	Dynamic	Calibration
Value	25 / 50 default (20 to 60 Ω w/ Ext R)	50 Ω	Turn R_t off during writes	R_s & R_t
Comment	All banks +/- 5%	All banks +/- 5%	Saves power (Also off during bus idle)	PVT compensation (requires external resistor)

* Stratix III FPGA also supports on-chip differential termination (covered earlier)

** Final values and tolerances pending characterization

Variable Input and Output Delay For Deskew

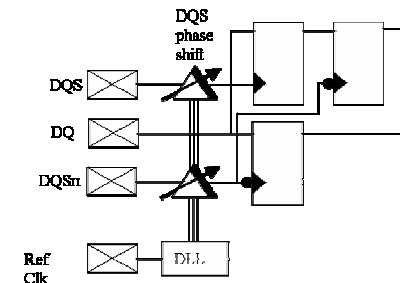
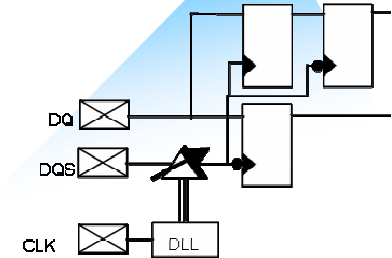
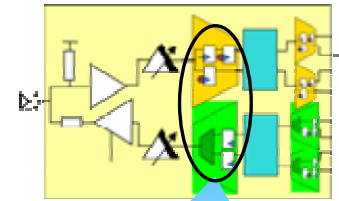


Path	Run-time configurable	Step size	Set at compile	Step size	Output buffer	Step size	Total
Input	1100 ps	50 ps	2800 ps	400 ps			3900 ps
Output	1050 ps	50 ps			150 ps	50 ps	1200 ps

Resolution and absolute value pending characterization

PVT-Compensated DQS Phase Shift

- DLL provides PVT compensation to DQS block
- DQS block phase shift incoming DQS
 - Non-intrusive to datapath
 - PVT compensated
 - Range of shifts of 0° to 180°
 - Phase shift independent of DQ de-skew
- 4-, 8-, 9-, 16-, 18-, 32-, or 36-bit programmable DQ group widths
- Use DQS only, DQS/DQSn differential or DQS and DQSn separately (e.g., QDR II+)
- 4 DLLs support multiple independent memory interfaces
 - Each DLL has two outputs
 - Each I/O bank can access 2 DLLs
 - Allows multiple interfaces, separate frequencies

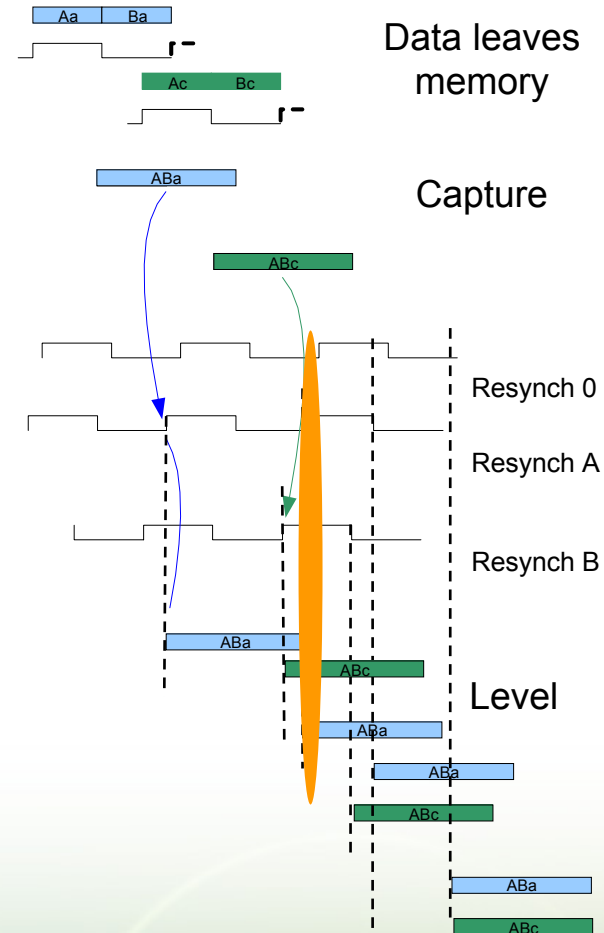
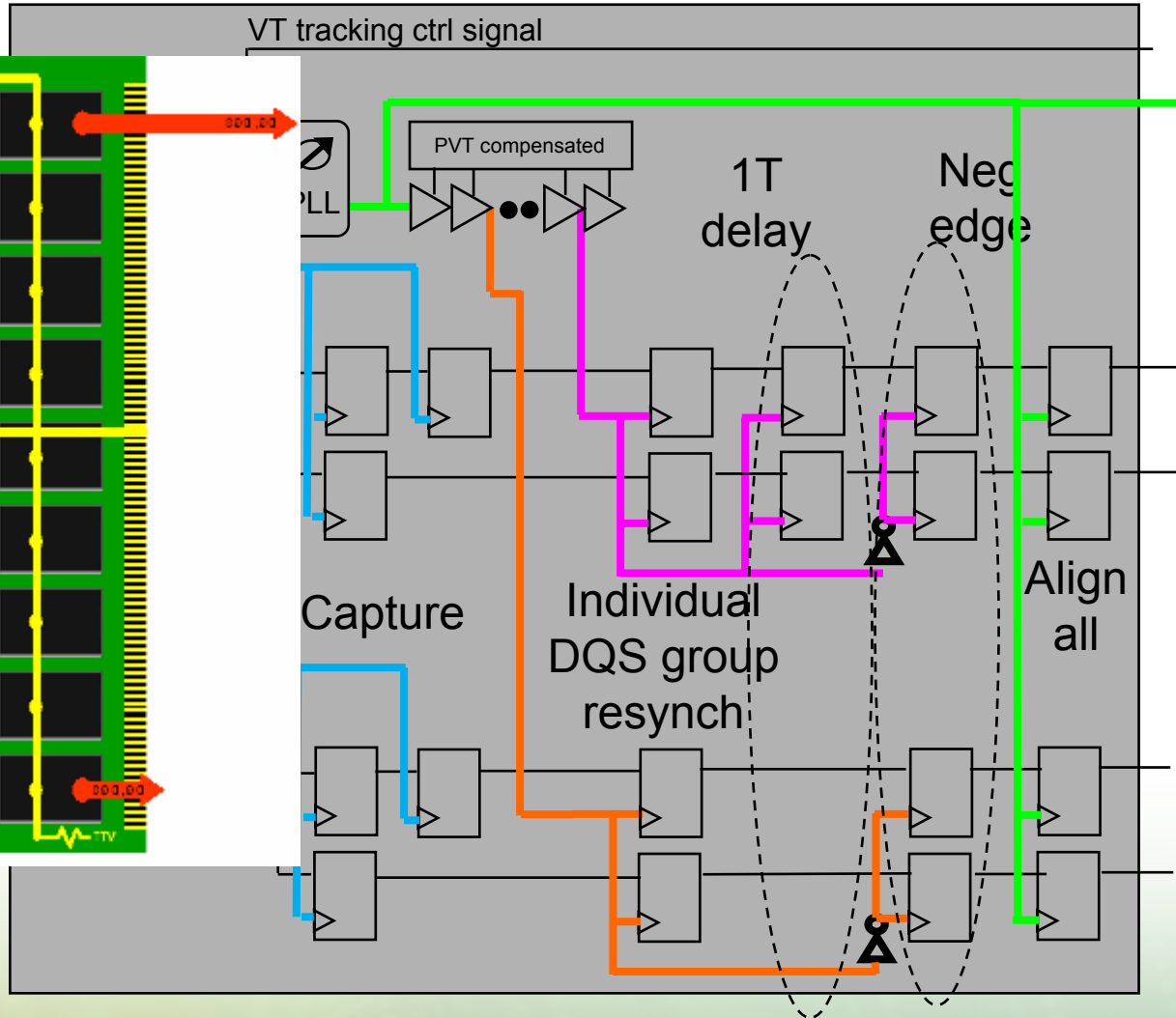
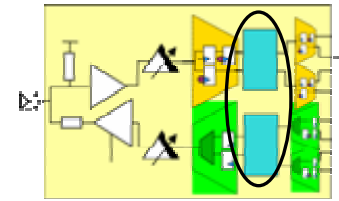




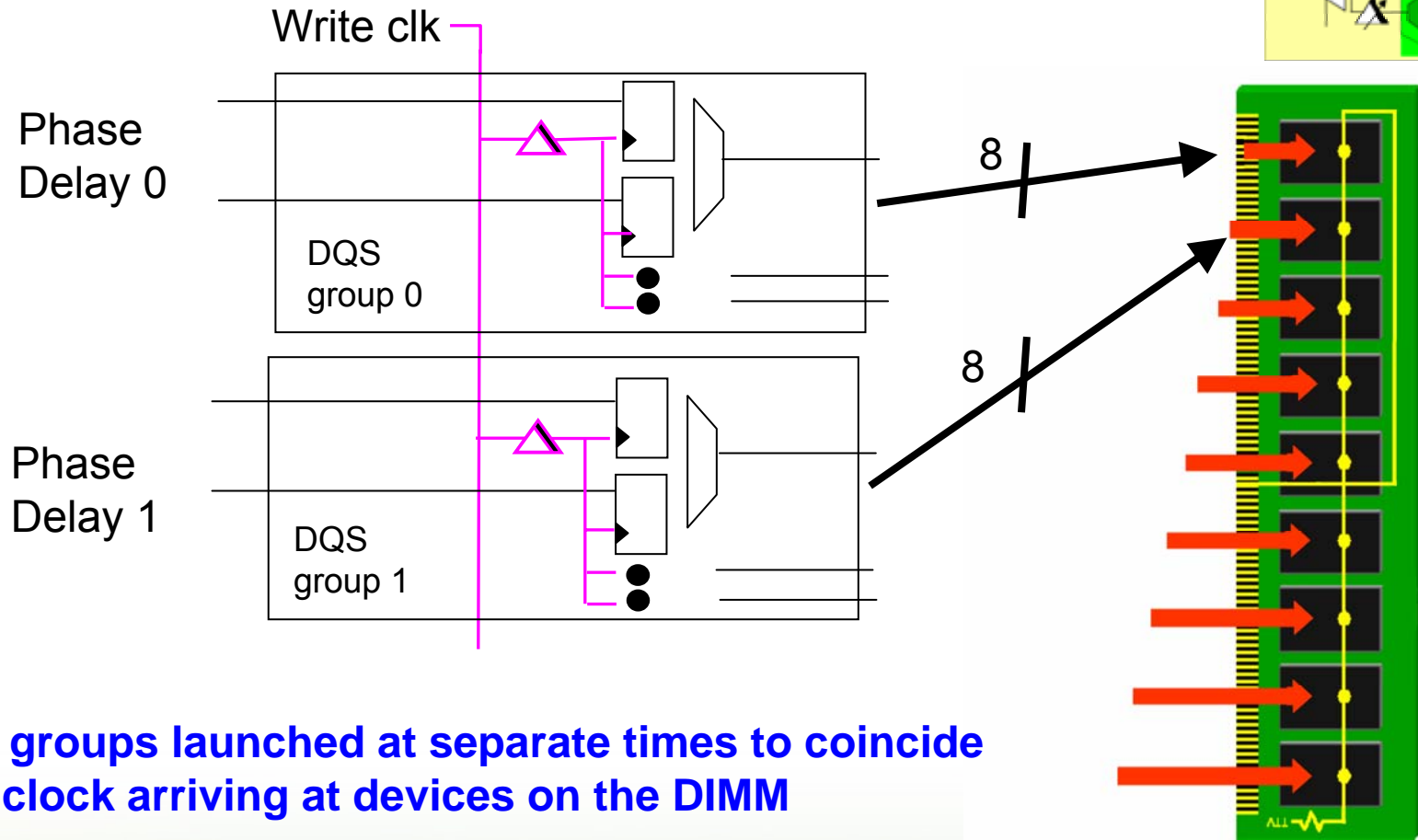
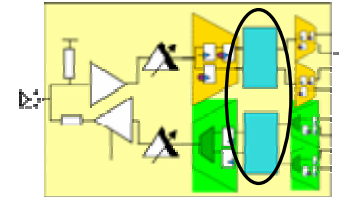
DDR3 Leveling in Stratix III FPGAs

Stratix III DDR3 Read Levelling

Stratix III I/O Block













Write Leveling Built Into I/O For DDR3



DQS groups launched at separate times to coincide with clock arriving at devices on the DIMM



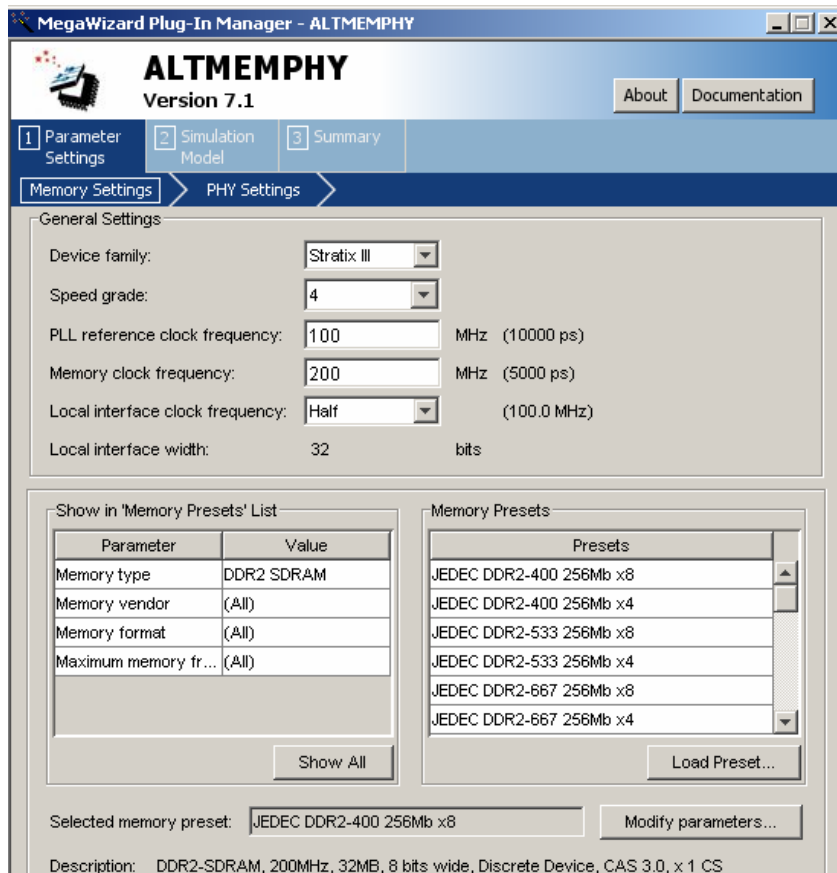
DDR3 Features

	Stratix III FPGA	Virtex-5	Comment
Variable I/O delay			Required for inter DQS group DQ deskew
PVT-compensated individual DQS group delay			Required for read and write leveling
1T delay registers			Required for read and write leveling
Neg edge registers			Required for read and write leveling
All contained directly in I/O			Reduces clock resources consumed, allows higher frequency of operation, saves cost of external components

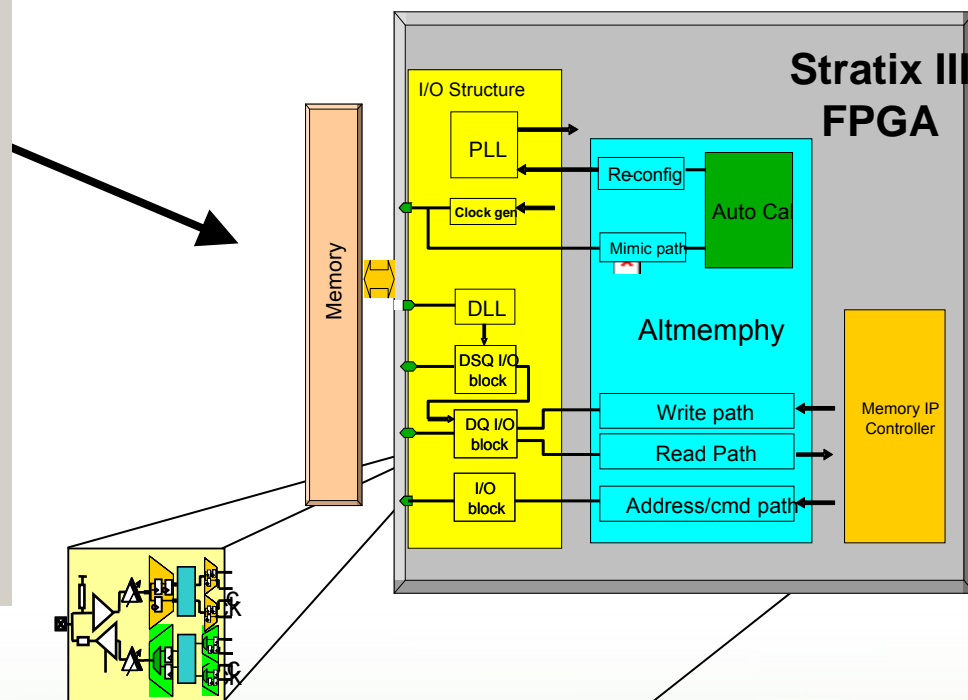


Software Tools

Adding the IP: GUI Tool For Rapid Integration



- Altmemory integrates PLL, DLL, DQS, and DQ hard macros



Altera or user-defined controller

■ Constrained with SDC

- Synopsys Design Constraints (SDC)
- Industry standard
- Easy to constrain data with respect to source synchronous clock

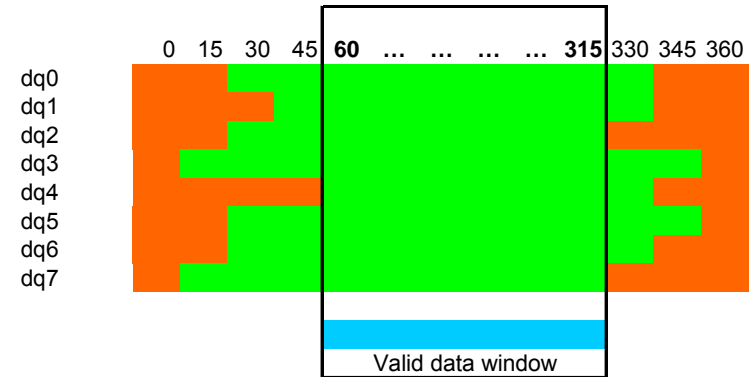
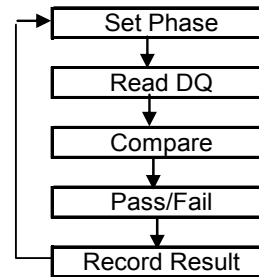
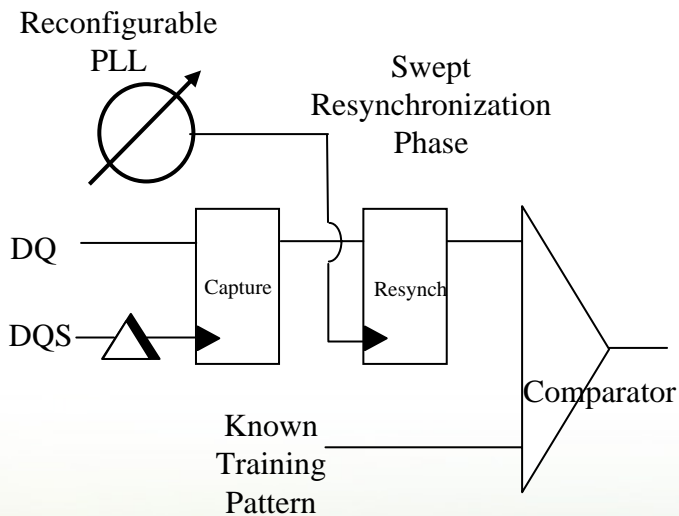
CY8

For graphic on right, need a noun after Stratix III per Altera trademark rules....You can have it say: Stratix III FPGA. (I can't edit this graphic)

Christine Young, 2007-8-24

Altmemory IP Calibration at Start-up

- Calibration – Removes process variation from FPGA and memory
 - Sweep all resynch phases for all DQ pins
 - Build map: pin-by-pin basis
 - Select best resynch phase



Ideal resynch phase: maximum setup and hold margin

Closing Timing On Source-Synchronous Interface With TimeQuest

- ASiC-strength timing analysis tool

The image displays several windows from the Quartus II software suite. The primary window is the TimeQuest Timing Analyzer, showing a path delay table with a total slack of 0.068 ns. A pie chart indicates that 49% of the delay is due to ICs and 51% is due to cells. Below this, a detailed data arrival path table is visible, listing elements like launch edge time, clock network delay, and various multiplexers and decoders. To the right, the Static Timing Analyzer Tool is open, showing a 'Report Timing' dialog box with fields for 'Paths to report' (set to 20) and 'From'/'To' nodes. A 'Clock Histogram' window is also present, showing a bar chart of delay distribution. At the bottom, a console window displays the command-line interface for running the timing analysis, including commands like 'create_clock', 'update_timing_summary', and 'create_slack_histogram'.

Property	Value
1 From Node	state_ni_inst18e_tapt
2 To Node	acc_inst8u[1]
3 Launch Clock	clk
4 Latch Clock	clk
5 Data Arrival Time	12.105
6 Data Required Time	12.233
7 Slack	0.068

Total	Incr	RF	Type	Fanout	Location	Element
0.000	0.000					launch edge time
2.277	2.277	R				clock network delay
2.450	0.173		u1co	1	LC_Q23_Y13_N9	state_ni_inst18e_tapt
2.450	0.000	RR	CELL	22	LC_Q23_Y12_N9	inst18e_tap4FREGOUT
5.283	0.443	RR	IC	1	LC_Q23_Y13_N1	inst18e_tap2_DUP_NODEEDATAC
3.118	0.225	RR	CELL	12	LC_Q23_Y13_N1	inst18e_tap2_DUP_NODECOMBOUT
4.650	0.932	RR	IC	1	LC_Q23_Y14_N3	inst8u_200COMBOUT
4.590	0.340	RR	CELL	2	LC_Q23_Y14_N3	inst8u_200COMBOUT
4.530	0.140	RR	IC	1	LC_Q23_Y14_N4	inst8m_ma_componentma_coredecoder_node110COMBOUT
4.618	0.088	RR	CELL	1	LC_Q23_Y14_N4	inst8m_ma_componentma_coredecoder_node110COMBOUT
11.556	0.930	RR	IC	3	LC_Q23_Y12_N0	inst8m_ma_componentma_compadderdecoder0addressm_nodes_bu160120DATA
12.599	0.443	RR	CELL	1	LC_Q23_Y12_N0	inst8m_ma_componentma_compadderdecoder0addressm_nodes_bu160120OUT1
13.566	0.000	RR	IC	2	LC_Q23_Y12_N1	inst8m_ma_componentma_compadderdecoder0addressm_nodes_bu160130CN1
14.647	0.458	RR	CELL	1	LC_Q23_Y12_N1	inst8m_ma_componentma_compadderdecoder0addressm_nodes_bu160130COMBOUT

```
Info: No PLL clocks were found without an assignment.
create_clock -period 10.000 -name clk [get_ports clk]
create_clock -period 10.000 -name clk2 [get_ports clk2]
Info: Quartus II 6.0 PVCS Trunk - quartus.sls
Info: Path #1: Slack is -2.222 (VIOLATED)
Info: From Node : time_c11time151
Info: To Node : time151
Info: Launch Clock : c11c2
Info: Latch Clock : c11c2
Info: Data Arrival Path:
Info: Total (ns) Incr (ns) Type Node
Info: 0.0000 0.0000 launch edge time
Info: 2.3977 2.3977 R clock network delay
Info: 2.4911 0.0934 u1co time_c11time151
Info: 2.4911 0.0000 FP CELL time_c11time151FREGOUT
Info: 3.1891 0.6189 FP IC time151DRAIN
Info: 5.2222 2.1211 FP CELL time151
Info: Data Required Path:
Info: Total (ns) Incr (ns) Type Node
Info: 0.0000 0.0000 launch edge time
Info: 2.0000 -2.0000 R clock network delay
Info: 3.0000 0.0000 u1su time151
Info: Data Arrival Time : 5.222
Info: Data Required Time : 3.000
Info: Slack : -2.222 (VIOLATED)
Info: c1c13
```

Read Timing Analysis – DDR3-800

Parameter	Timing without calibration (ps)*	Timing with calibration (ps)*	Description
Period	2,500	2,500	400 MHz
t_{HP}	1,250	1,250	Ideal half period time
DRAM uncertainties	500	200	DQ-DQ and DQS-DQ skew reduced via deskew
T_{DCD}	125	125	FPGA output clock duty cycle distortion ($\pm 5\%$)
FPGA + board uncertainties	550	300	Uncertainties include DLL jitter, setup and hold, clock tree skew, SSI jitter
Margin	75	625	Read timing margin

Write Timing Analysis – DDR3-800

Parameter	Timing without calibration (ps)*	Timing with calibration (ps)*	Description
t_{HP}	1,250	1,250	Ideal half period time
DRAM uncertainties	425	200	DQ-DQ and DQS-DQ skew reduced via deskew
T_{DCD}	125	125	FPGA output clock duty cycle distortion ($\pm 5\%$)
FPGA + board uncertainties	575	300	Uncertainties include PLL jitter, clock network skew, PRBS data pattern jitter, rise/fall mismatch, and SSO pushout
Margin	125	625	Write timing margin

Performance Summary

- Performance shown for 1.1V core
- Frequency of operation is **expected to go up** post characterization

Memory standards	I/O standards	-2 speed grade (MHz)		-3 speed grade (MHz)		-4 speed grade (MHz)		Maximum data rate
		Column I/Os	Row I/Os	Column I/Os	Row I/Os	Column I/Os	Row I/Os	Fastest speed
DDR SDRAM	SSTL-2	200	200	200	200	200	200	400 Mbps
DDR2 SDRAM	SSTL-1.8	400	300	333	267	333	267	800 Mbps
DDR3 SDRAM	SSTL-1.5	400	300	333	TBD	333	TBD	800 Mbps
RLDRAM II	1.8V HSTL	400	300	300	250	300	250	800/1,600 Mbps
QDR II SRAM	1.8V and 1.5V HSTL	350	300	300	250	300	250	1,400 Mbps
QDR II + SRAM	1.8V and 1.5V HSTL	350	300	300	250	300	250	1,400 Mbps

The Only FPGA with DDR3 Support



Conclusion

- Stratix III FPGAs offer the highest reliable frequency of operation across PVT
 - DQ/DQS block
 - Dynamic calibration with PVT compensation
 - Deskew feature
- Stratix III FPGAs are the only FPGAs to offer DDR3 memory interface support
 - Includes support for DDR3 DIMMs



Thank You!