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## Lab 6: Transistor sizing supplement

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Consider a 2-input NAND gate driving a load. It is required that the transistors of the 2-input NAND gate be sized such that the propagation delays from the input to the output match that for a simple inverter driving the same load for output rising as well as falling.

The size of the inverter is fixed by the load it needs to drive. Consider that an inverter of width ratio  $W_{\text{pmos}}/W_{\text{nmos}}$  is required to drive the load. To determine the sizes of the transistors for an “equivalent NAND gate” to drive the same load we proceed as follows:

The 2-input NAND gate has two PMOS transistors in parallel for the pull-up network and two NMOS transistors in series for the pull-down network.

For the pull-up network, the worst case  $t_{\text{rise}}$  would be when only one of the two pull-up transistors is 'on'. So for the  $t_{\text{rise}}$  of worst case pull-up to be comparable to that of the inverter, each of the PMOS transistors in the NAND gate should have the same size as the PMOS transistor in the inverter.

$$\text{thus } W_{\text{pmos NAND}} = W_{\text{pmos inverter}}$$

For the NAND gate to pull-down, both the NMOS transistors need to be 'on'. It can be seen that if each of the NMOS transistors has the same size as that for the inverter, the  $t_{\text{fall}}$  for the NAND gate would be twice that for the inverter. This is because there is a delay of  $R_{\text{on}} \cdot C_{\text{load}}$  ( $R_{\text{on}}$  is 'on' resistance) introduced by each of the two series NMOS transistors in the NAND gate. So to get comparable fall time, the  $R_{\text{on}}$  of the two transistors in series in the NAND gate should equal the  $R_{\text{on}}$  of the pull-down NMOS transistor in the inverter.

$R_{\text{on}}$  is inversely proportional to the  $W/L$  ratio of the transistor. Therefore increasing the width  $W$  of the transistor decreases the on resistance provided the length  $L$  remains the same. Thus each of the two series NMOS transistors in the NAND gate should have half the  $R_{\text{on}}$  associated with the inverter NMOS transistor. This means that the NMOS transistors in the NAND gate should have aspect ratios  $2W_{\text{nmos}}/L$  ( $W_{\text{nmos}}/L$  is the aspect ratio of NMOS transistor of the inverter).

$$\text{thus } W_{\text{nmos NAND}} = 2 W_{\text{nmos inverter}}$$

A similar procedure can be used to size other complex gates as well. For complex gates there may exist several pull-up/pull-down paths. Sizing should be done for all the different pull-up/pull-down paths. If a transistor is a part of more than one pull-up/pull-down path, then fix the size of that transistor based on one path first, and then work out the sizes for the other transistors in the remaining paths.

$W_{\text{nmos}}$  of the reference inverter is given as  $1.2u$ . From Part B obtain  $W_{\text{pmos}}$  such that the rise/fall times are comparable. Once you obtain  $W_{\text{pmos}}$  to satisfy this constraint, the width ratio  $W_{\text{pmos}}/W_{\text{nmos}}$  of the reference inverter is known.

Size the complex gate in Part C so that the rise/fall times will be comparable to that when the reference inverter drives the same load.

To compute the worst case rise/fall time for the complex gate, identify the longest path first. For measuring the rise time, have all the inputs except one at logic low (on the longest path). Then make the high input go low and measure the rise time from input going low to output going high. Similarly for fall time measurement, need to have all the inputs except one at logic 'high'. Then make the low input go high and measure the fall time from input going high to output going low. Use 30%–70% delay times. Depending on which transistor in the pull-up/pull-down path switches, there will be slight differences in the rise/fall times. For this lab, switch the transistor that is closest to the output on the longest path.