TEMIC Semiconductors

MATRA MHS

TEMIC ICs RISC processors roadmap

## Dominique de Saint Roman

ESTEC ERC32 Evaluator Workshop
January 28, 98

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TEMIC
S e m i c o n d u c t o r s

Current ERC32 status

- built with 3 chips:
  - ▶ the Integer Unit (IU/TSC691E, rev C)
  - ▶ the Floating Point Unit (FPU/TSC692E, rev B)
  - ▶ the MEmory Chip (MEC/TSC693E, rev A)
- rev H set of specifications available on ESTEC and TEMIC webs
- rev I set of specifications will be released end of february 98
- 10 MIPs @ 14 MHz
- 2.5 W @ 10 MHz
- latch immune
- total dose better than 50 Krads
- SEU threshold better than 15 MeV
- more than 99 % SEU induced errors detected and trapped
- available up to SCC quality grades
- designed mostly on ISS (DMS-R and ERA)

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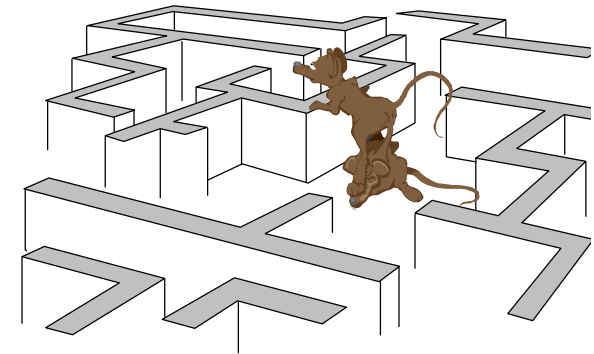
Current activities
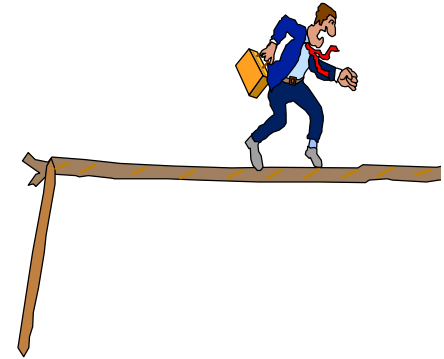
- ● FPU rev B redesign:
  - ► fixes all specification non conformities identified as off december 19, 97:
    - − these identified during applications designs
    - − these detected during redesign
    - − all listed in the design considerations document issued december 19, 97
  - ► tape out done early january 98
  - ► fab out scheduled early february
  - ► final validation scheduled for end of april 98
 - ► meanwhile, we keep delivering rev B

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Current activities (cont'd)

- ● ERC32 MCM:
  - ► joint MMS and TEMIC development
  - ► will be marketed and sold by TEMIC
  - ► integrates:
    - − ERC32 IU, FPU and MEC chips
    - − DMA I/F
    - − RAM I/F
    - − 8 bit data ROM I/F
    - − IO I/F
    - − external interrupt I/F
    - − UART I/F
  - ► packaged into a dual use package: MQFPF and BGA
  - ► allows more than 25% board saving (package body size is 51x59 mm)
  - ► will be sampled end of 2Q98
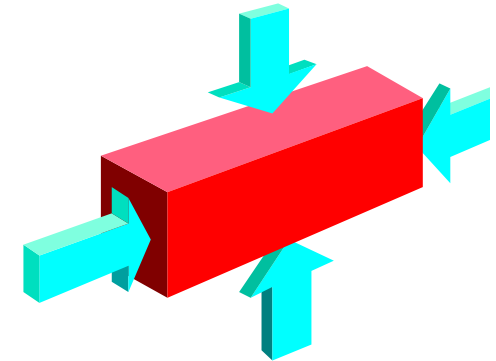 - ► will be made available to mil qual grades only, on a first place
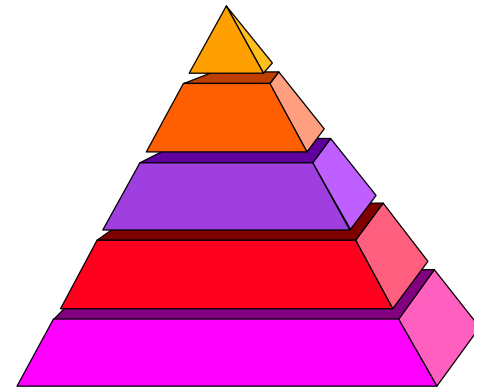
Current activities (cont'd)

- ● ERC32 Single Chip (SC):
  - ► straight forward integration of existing IU, FPU and MEC chips on 0.5 µm CMOS RTP process
  - ► resulting chip package pinout compatible with existing MEC
  - ► we are also trying to make resulting chip frame and pad signal assignment compatible with existing MEC chip (optional)
  - ► expected resulting performances:
    - − 25 MIPs @ 35 MHz & 5 V
    - − 2.5 W @ 35 MHz
    - − 3 V +/-10% spec for power saving
    - − latch up immune and SEU threshold better than 50 MeV
    - − total dose better than 100 Krads
  - ► design start early february
  - ► tape out 4Q98
  - ► validation 2Q99
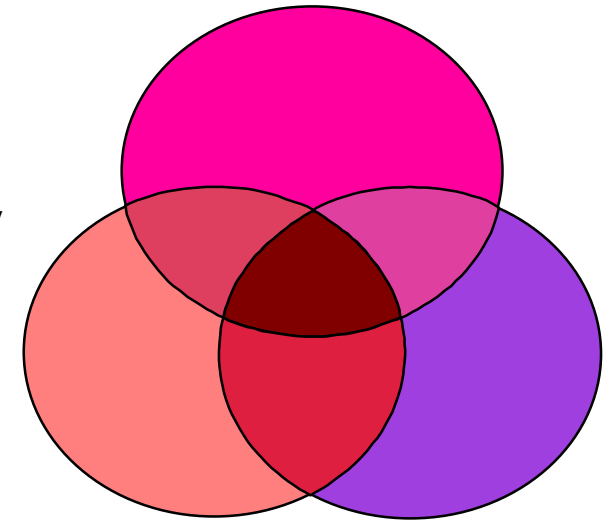
Current activities (cont'd)

- ● ERC32 New Generation (NG):
  - ► definition questionnaires distributed throughout the world
  - ► Tharsys will evaluate the answers and make a definition proposal
  - ► type of evolutions:
    - − V7 / V8
    - − data/instruction caches
    - − processor buses: PCI, VME,...
    - − specific memory I/F (RAM, ROM, DRAM, SDRAM,...)
    - − specific I/F: 1553, RS232, RS422...
  - ► considering integration on 0.35 µm CMOS RT process
  - ► TEMIC / THARSYS specification proposal end of 1Q98
  - ► proposal submission to ESTEC mid 98
  - ► kick off end of 98
  - ► chip validation mid 2000

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Resulting RISC processors roadmap

MIPs

ERC32NG

25

ERC32SC

MCM ERC32
ERC32(C, C, A)

10

ERC32(C, B, A)

1997   1998   1999   2000   2001