Stratix FPGA Homework

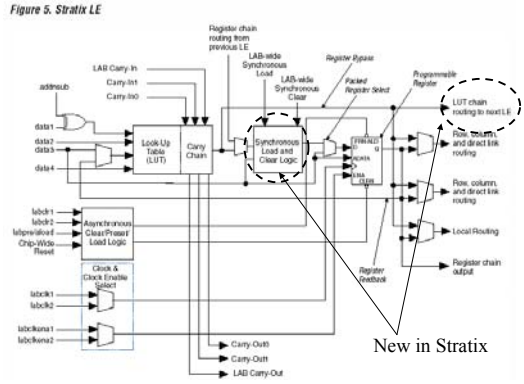
Compare Altera Stratix and FLEX families in several areas.

Basic mechanism for implementing random logic is the Logic Element which contains a 4-input Lookup Table + DFF.

This has not changed much between families.

One difference is that Stratix added synchronous load and clear logic to every LE; this is a common functionality to have in register which was implemented as part of the LUT4 logic in the FLEX10K.

Also, old 'cascade' function in FLEX for wide AND/OR functions generalized in Stratix by allowing LUTs to chained together for wide functions (chain input is dedicated route between logic elements).



Fast Addition/Subtraction

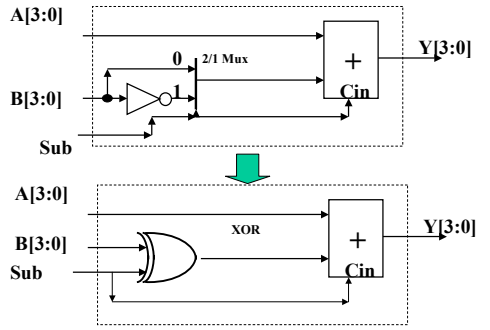
Fact: The speed of carry generation determines speed of adder for binary addition.

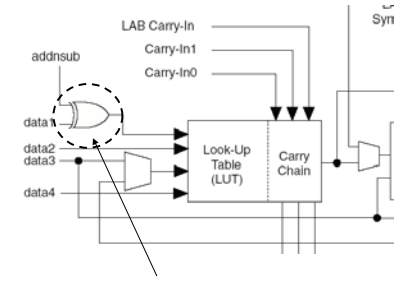
FLEX10K had carry logic in each LE and dedicated carry chain routing between LEs to speed up carry propagation so that LUT4 and programmable routing did not have be used for carry logic.

Stratix does several things to make addition and adder/subtractor faster and more efficient.

Adder/Subtractor Operation

A – B = A + B' + 1



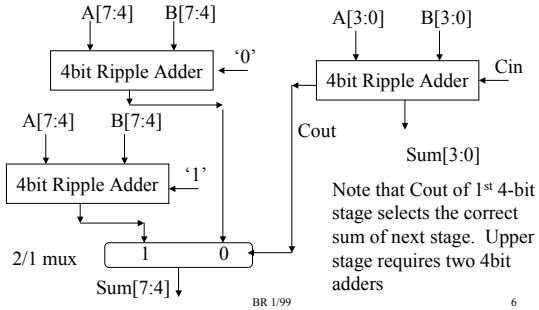


New to Stratix LE.

Used for building adder/subtractor, do not have to use LUT logic for this -- will speed up the operation and be more efficient in terms of resource usage.

Carry-Select Adder

The Carry path is the slowest path in the ripple carry adder. We can speed it up with the following scheme (8-bit adder):



Note that Cout of 1st 4-bit stage selects the correct sum of next stage. Upper stage requires two 4bit adders

Carry-Select Adder (larger N)

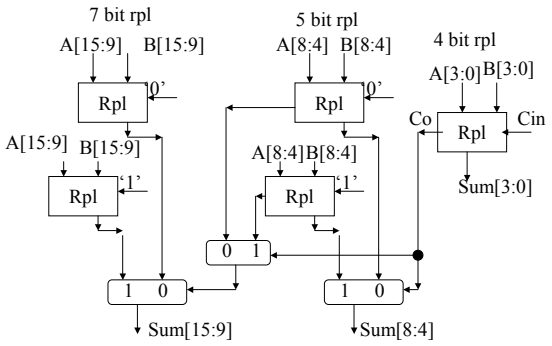
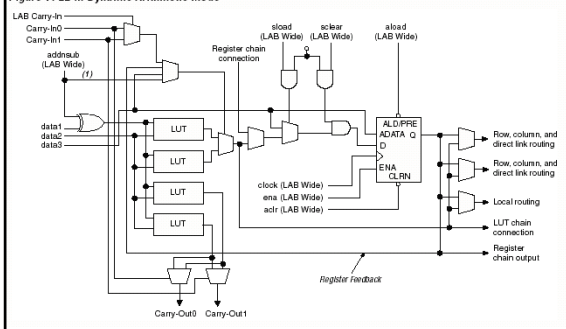
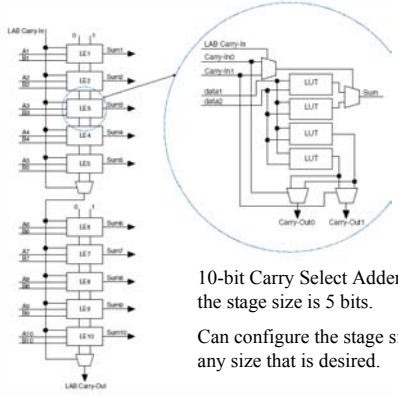


Figure 7. LE in Dynamic Arithmetic Mode



Note that in this mode, LUT4 split into four 2-input LUTs, for computing sum bits with carry-in = 0,1 and computing carry outs for carry-in = 0,1



10-bit Carry Select Adder – note that the stage size is 5 bits.

Can configure the stage size to be any size that is desired.

Higher Level Arithmetic Support

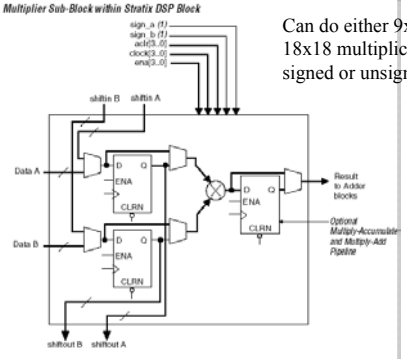
Flex10K had no support for higher level arithmetic support other than implementation as a netlist of LUT4s.

Stratix has monolithic multipliers which can be configured as 9x9 or 18x18 multipliers. Four 18x18 multipliers can be used with a dedicated adder to form a 36x36 multiplier.

Multiplier sub-blocks are embedded in a DSP block. Output of multipliers to adder block that can be used for accumulation.

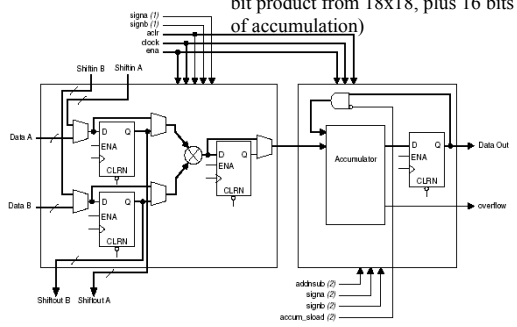
An interesting omission is that the DSP block cannot do saturating arithmetic.

Figure 32. Multiplier Sub-Block within Stratix DSP Block



Can do either 9x9 or 18x18 multiplication, signed or unsigned.

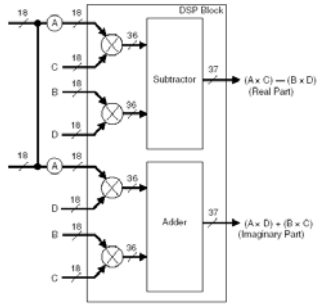
Figure 37. Multiply-Accumulate Mode



Accumulator can be up to 52 bits (36 bit product from 18x18, plus 16 bits of accumulation)

$$(a + jb) \times (c + jd) = [(a \times c) - (b \times d)] + j \times [(a \times d) + (b \times c)]$$

Figure 38. Two-Multipliers Adder Mode Implementing Complex Multiply



Summary of DSP Block Modes

Table 20. Multiplier Size & Configurations per DSP block

DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	Two multiply and accumulate (52 bits)	Two multiply and accumulate (52 bits)	–
Two-multipliers adder	Four sums of two multiplier products each	Two sums of two multiplier products each	–
Four-multipliers adder	Two sums of four multiplier products each	One sum of four multiplier products each	–

SRAM Comparison

Flex10K: 2Kb single port SRAM blocks, configured as 256x8, 512x4, 1024x2, or 2048 x 1 . Any dual port SRAM support is strictly multi-cycle dual port SRAM.

Stratix: three different blocks sizes available 512b, 4Kb, and one large block whose size is dependent upon the part.

True Dual Port SRAM available.

Table 7. TriMatrix Memory Features

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	MegaRAM Block (4K × 144 Bits)
Maximum performance	312 MHz	312 MHz	300 MHz
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Byte enable		✓	✓
Parity bits	✓	✓	✓
Shift register	✓	✓	
Mixed clock mode	✓	✓	✓
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

In dual port modes, widths of the ports can be different

True dual port – any combination of reads/writes on ports at same/different clock frequencies

Figure 12. True Dual-Port Memory Configuration

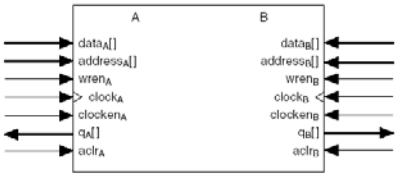
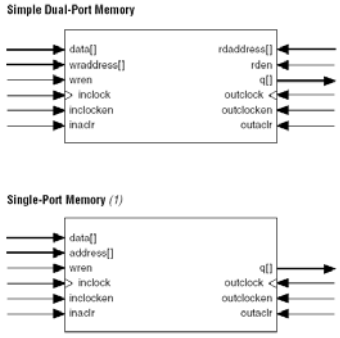


Figure 13. Simple Dual-Port & Single-Port Memory Configurations



Simple Dual-port – only support read and write in same clock cycle.

Good for FIFOs.

Clocking Comparison

Flex 10K: each LE can select 1 of 2 global clocks. PLL provides clock multiplication by 2, and also syncs internal clock edges to external clock edges.

Stratix: Hierarchical clocking scheme, 16 global clock networks, driven by 4 enhanced PLLs. 16 regional clocks (4 per device quadrant), and 8 dedicated fast regional clock networks.

Clock Frequency Scaling: m/(n * post-scale counter) where m,n , post scale counter all go from 1 to 512. M, N used for clock frequency, post-scale counter controls duty cycle.

Clock Skew

We have used the equation:

reg-to-reg delay = C2q + MaxCombDelay + Tsu

It is actually:

reg-to-reg delay = C2q + MaxCombDelay + Tsu + Tskew

Where Tskew is the clock skew. Clock skew is the difference in arrival times of clock edges at DFFs on the device.

Tskew is determined by die size, propagation delay across chip. Gate delays used to be large compared to Tskew, so could ignore. As transistor lengths have scaled down, gates have gotten faster and can no longer ignore Tskew.

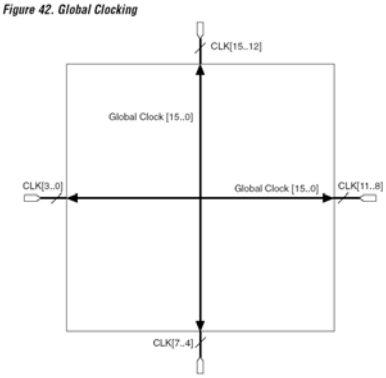
Why Hierarchical Clocks?

Why have global, regional and fast regional clocks?

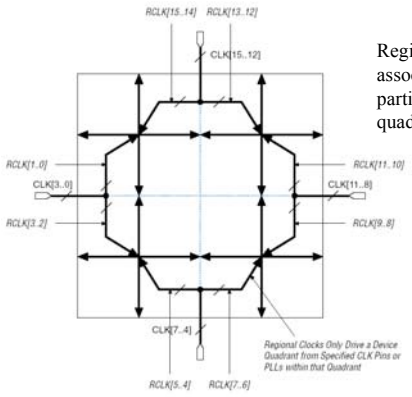
Because can specify different skews on the two clock networks – regional clocks will have smaller skew than global clocks, so any register-to-register paths clocked only by a regional clock can have tighter timing than a register to register path that crosses a regional boundary.

Can also save power

Figure 42. Global Clocking

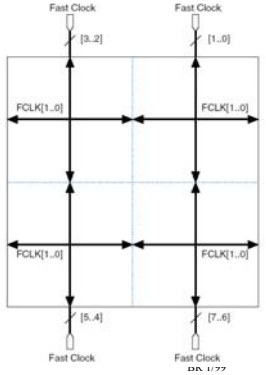


Can be used for any clocking source



Regional clocks are associated with a particular chip quadrant.

Fast Regional Clocks



Suggested uses for fast regional clocks are high fanout signals like synchronous loads/clears, clock enables.

IO Technology

- Input/Output (IO) has become very complex
  - Used to only have to worry about TTL vs CMOS
  - TTL had current drive requirements, CMOS just voltage level requirements
  - Both used full swing signals (0 to Vdd, used to be 5 V)
- New issues in IO technology
  - Limit voltage swing to speed up signaling
  - Voltage swing about a reference voltage instead of between 0 and Vdd
  - Differential signaling to reject noise
  - Termination required to prevent signal reflections from corrupting signals

Stratix supported IO standards

Table 28. Stratix Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL	Differential	N/A	1.5	N/A
Differential SSTL	Differential	N/A	2.5	N/A
GTL / GTL+	Voltage-referenced	1.0	N/A	1.5
HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage-referenced	1.5	3.3	1.5
AGP (1× and 2×)	Voltage-referenced	1.32	3.3	N/A
CTT	Voltage-referenced	1.5	3.3	1.5

Classification of Advanced IO standards

- Single Ended- Full swing signals between 0 and VCCIO, tolerant of overdrive of input signals, various current drive capability
  - LVTTL, LVCMOS -- tolerant of 5V overdrive, expects 3.3 V
  - 2.5V, 1.8V, 1.5V – simply lower voltage versions of LVTTL, LVCMOS
  - PCI 3.3V, PCI-X 3.3V – expects 3.3 V input signals, used to limit signal overshoot. But makes the pin intolerant of any drive that is over the clamping limit unless external series resistor used to limit current.

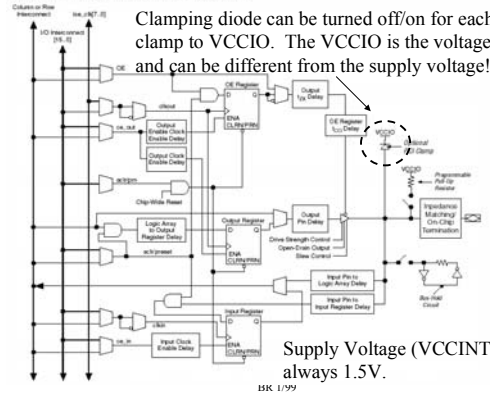
Table 32. Stratix MultiVolt I/O Support *Note (1)*

VCCIO (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8		✓	✓	✓		✓ (2)	✓			
2.5			✓	✓		✓ (3)	✓ (3)	✓		
3.3			✓	✓	✓ (4)	✓ (5)	✓ (5)	✓ (5)	✓	✓

Notes to Table 32:

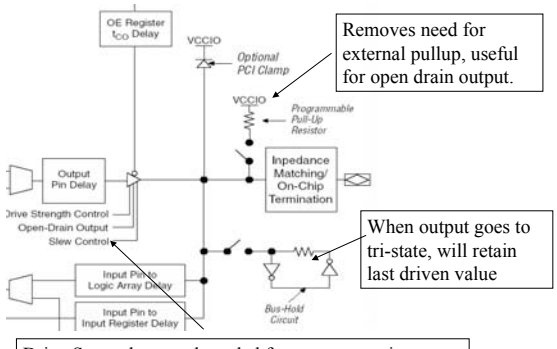
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
(2) When V_{CCIO} = 1.8 V, a Stratix device can drive a 1.5-V device with 1.8-V tolerant inputs.
(3) When V_{CCIO} = 2.5 V, a Stratix device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(4) Stratix devices can be 5.0-V tolerant with the use of an external resistor and internal PCI clamp diode.
(5) When V_{CCIO} = 3.3 V, a Stratix device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Figure 63. Stratix IOE in Bidirectional I/O Configuration



Clamping diode can be turned off/on for each IO, clamp to VCCIO. The VCCIO is the voltage of IO, and can be different from the supply voltage!!!!

Supply Voltage (VCCINT) always 1.5V.



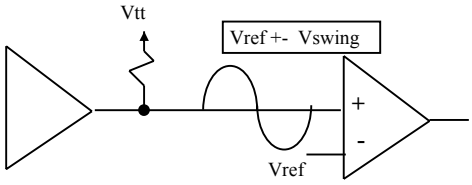
Removes need for external pullup, useful for open drain output.

When output goes to tri-state, will retain last driven value

Drive Strength control needed for current requirements of different IO standards

Classification of Advanced IO standards (cont)

- Voltage Referenced - Reduced voltage swing signals with differential receiver that compares input signal versus a reference voltage (Vref) . Requires termination resistor tied to Vtt.



Vswing usually 10's of millivolts to a few hundred millivolts. Vtt can be external to Receiver or internal. Vref can be supplied external or internal.

Why Voltage Referenced Signaling?

Smaller voltage swing means faster signaling.

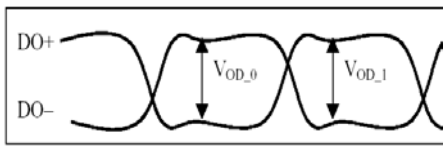
Smaller voltage swing also means less current drive required.

Can be susceptible to noise.

Gunning Transceiver Logic (GTL) is one of the supported standards, used on the Pentium III/III/IV busses. Vtt = 1.5v, Vref = 1.0, voltage swing is +/- 200 mv about Vref.

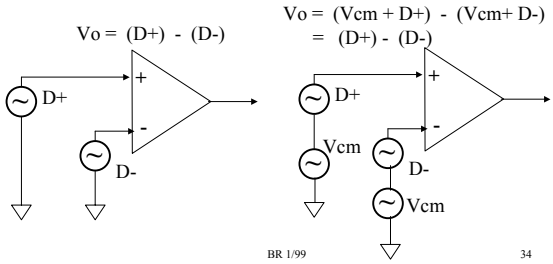
Classification of Advanced IO standards (cont)

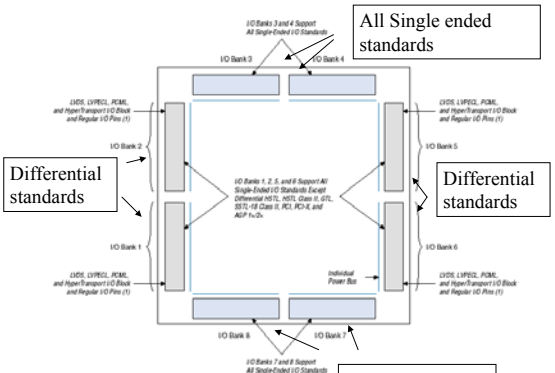
- Differential – two pairs of wires used to send a '1' or '0' – when D0+ > D0-, then a '1' level. When D0+ < D0-, then a '0' level. Typical differences in are in the few hundred millivolts.

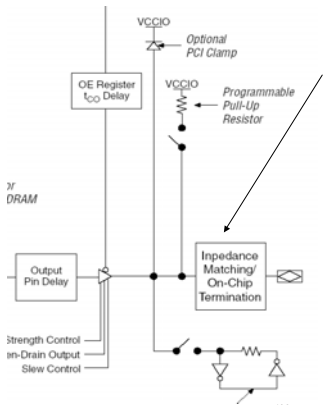


Why differential signaling??

Differential signaling very good at rejecting common-mode noise. If noise is coupled into a cable, then usually it is coupled into all wires in the cable. This 'common-mode' noise (Vcm) can be rejected by input amplifier.







On Chip Termination

High speed signaling can cause reflections if line is not properly terminated (termination impedance matches source impedance).

Rule of thumb: Reflections a problem when rise/fall time of signal is greater than 1/2 signal propagation delay along wire.

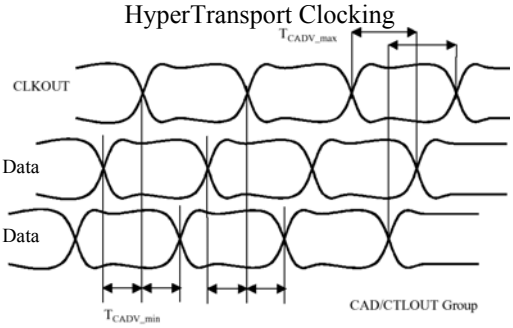
HyperTransport Differential Standard

HyperTransport is one of the supported differential standards. Each data line is actually a pair of lines.

HyperTransport uses a *source-synchronous* protocol – a clock is transmitted along with the data. The clock is differential, same as the data.

Speeds are 400 MT/s (million transfers), 600 MT/s, 800 MT/s, 1.0 GT/s, 1.2 GT/s, 1.6 GT/s. Bits/sec depends on number of data lines.

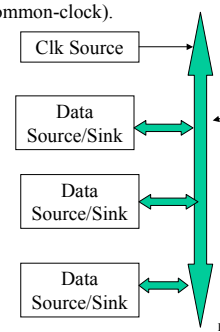
HyperTransport Clocking



Clock delayed by ½ bit time, so just latch data on crossing of clock signals. Valid data on CAD lines at clock crossings.

What is source-synchronous?

Traditional Synchronous (common-clock).



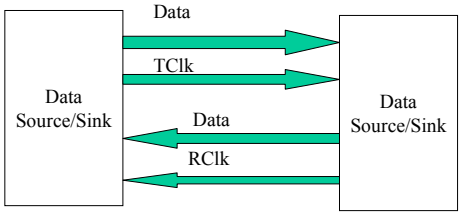
Backplane bus

Clock source comes from one global location, receiver/transmitter share the same clock.

Clock edge has different arrival times at data source/sinks due to different interconnect lengths (clock skew).

Setting worst case allowable clock skew limits interconnect length.

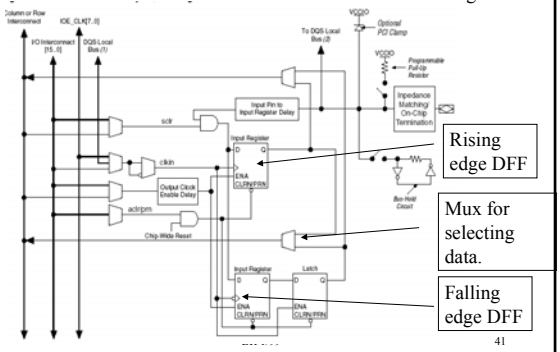
What is source-synchronous? (cont.)



Clock sent with data. Interconnect length does not matter because data, clock travels same distance and arrives at same time.

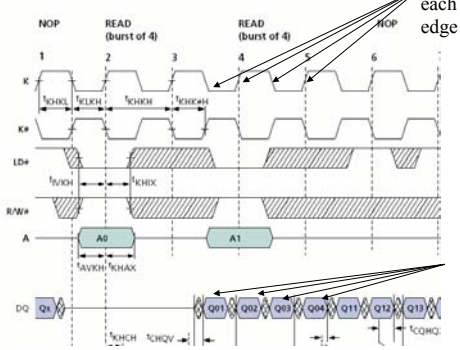
Double Data Rate Support

Double Data Rate interfaces transfer data on both clock edges.



SSRAM, SDRAM both have DDR varieties

Transfer on each clock edge



Micron DDR SSRAM

Data

Flex vs. Stratix: Key Differences

- Logic Element: Synchronous clr/preset built in, generalized cascade
- Addition/Subtraction: carry-select adder support, subtraction support in LE with XOR gate
- Other arithmetic: monolithic multipliers, DSP blocks with monolithic multipliers + adder for efficient multiply accumulate, multiply-sum
- SRAM: true dual port capability.
- Clocking: Hierarchical clock network with three levels of clocking (global, regional, fast regional)
- IO – support for new voltage-referenced and differential standards.

Altera Stratix vs. Xilinx Virtex II

- Logic elements are equivalent
- Virtex does not have carry-select adder support
- Virtex has monolithic multipliers (only 18x18 signed), but not DSP blocks (monolithic adder).
- Virtex does not have hierarchical clock network
- Both have true dual port RAM
- Both support the same IO standards.