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Appendix B HDL Entry—Tutorial 2

VHDL and Verilog are two main hardware description languages (HDL) for describing the behavior of a digital circuit. This tutorial provides a step-by-step instruction for either VHDL or Verilog text entry, followed by synthesis, and simulation of a 4-bit binary counter circuit. However, no knowledge of VHDL or Verilog is required to follow this tutorial. Tutorial 3 in Appendix C will show how this circuit can be downloaded to the PLD on the UP2 development board so that you can actually see this circuit executing in the hardware.

This tutorial is very similar to Tutorial 1 in Appendix A for schematic entry. The main difference is in using the Text Editor rather than the Graphic Editor. The procedures for project creation, synthesis, and simulation are the same in both cases. Even if you do not intend to write VHDL or Verilog code, you should go through this tutorial so that you can continue on to Tutorial 3 in Appendix C, and learn how to download a circuit to the PLD on the UP2 development board.

This tutorial assumes that you are familiar with the Microsoft Windows environment, and that the Quartus II software has already been installed on your computer. Instructions for the installation of the Quartus II software can be found on the CD-ROM. You also must obtain a free license file from the Altera website in order for the software to function correctly.

B.1 Getting Started

B.1.1 Preparing a Folder for the Project

1. Each circuit design in Quartus II is called a project. Each project should be placed in its own folder, since the synthesizer creates many associated working files for a project. Using Windows' File Manager, create a new folder for your new project. This tutorial uses a folder called `counter` created in the root directory of the C drive.
2. All of the Verilog source codes are located on the accompanying CD-ROM in the directory `Verilog Examples`, and all of the VHDL source codes are located in the directory `VHDL Examples`. The Verilog or VHDL source code for the counter circuit that we will be using for this tutorial is in the file
`<CD-ROM drive>:\Verilog Examples\Appendix B HDL Entry Tutorial 2\Source\counter.v`
or
`<CD-ROM drive>:\VHDL Examples\Appendix B HDL Entry Tutorial 2\Source\counter.vhd`
respectively.
3. Using Windows' File Manager, copy either the Verilog file `counter.v` or the VHDL file `counter.vhd` to the new folder `c:\counter` that you have created in Step 1. For the remainder of this tutorial, we will assume that you are using the Verilog file `counter.v`.

B.1.2 Starting Quartus II

After the successful installation of the Quartus II software, there should be a link to the program under the Windows' **Start** button. Click on this link to start the program. You should see the main Quartus II window similar to Figure B.1.

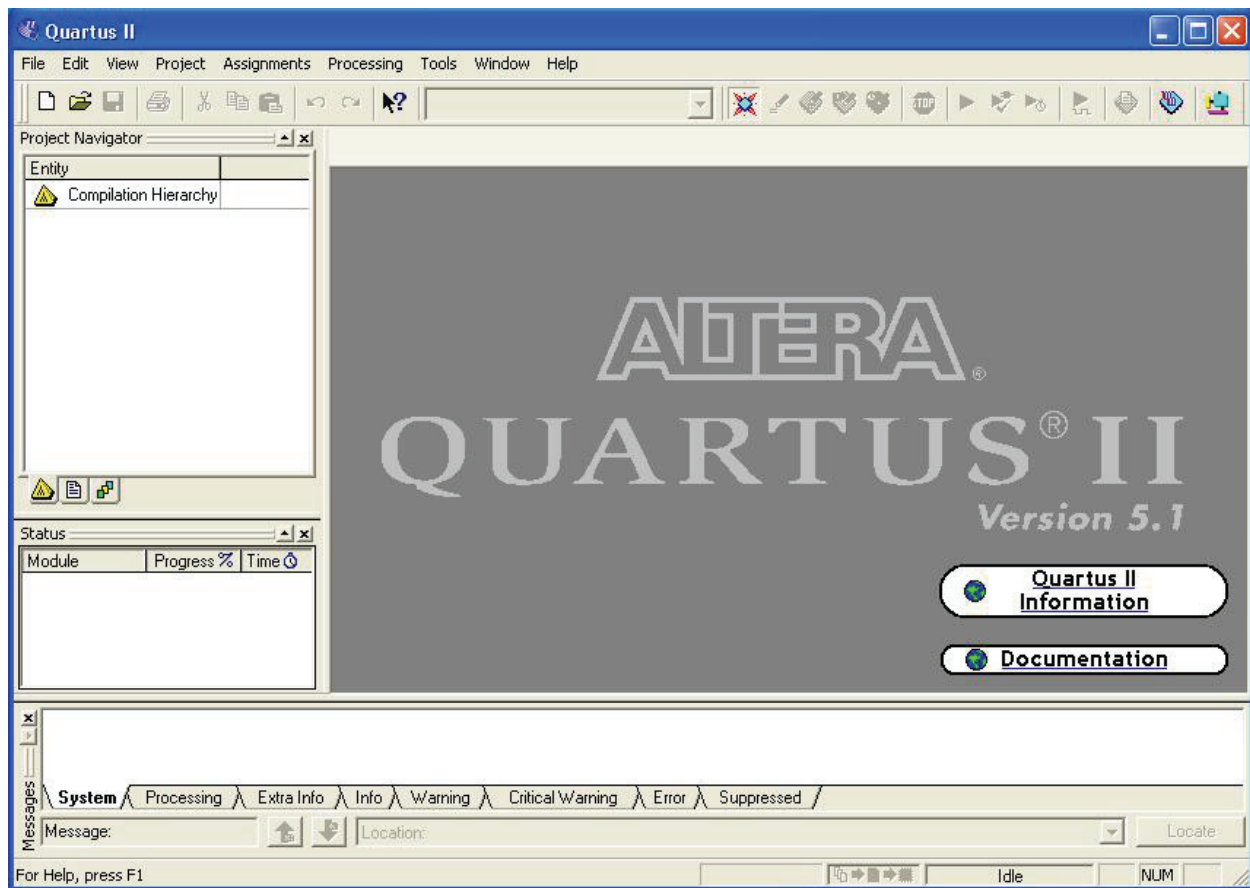


Figure B.1 The Quartus II main window.

B.1.3 Creating a New Project

Each circuit design in Quartus II is called a project. Each project should be placed in its own folder, since the program creates many associated working files for a project. Perform the following steps to create a new project to be stored in the folder that you have created in Section B.1.1.

1. From the Quartus II menu, select **File | New Project Wizard**, and then click **Next** to skip the new project wizard introduction message if it appears. You should see the New Project Wizard: Directory, Name, Top-Level Entity [page 1 of 5] window shown in Figure B.2.

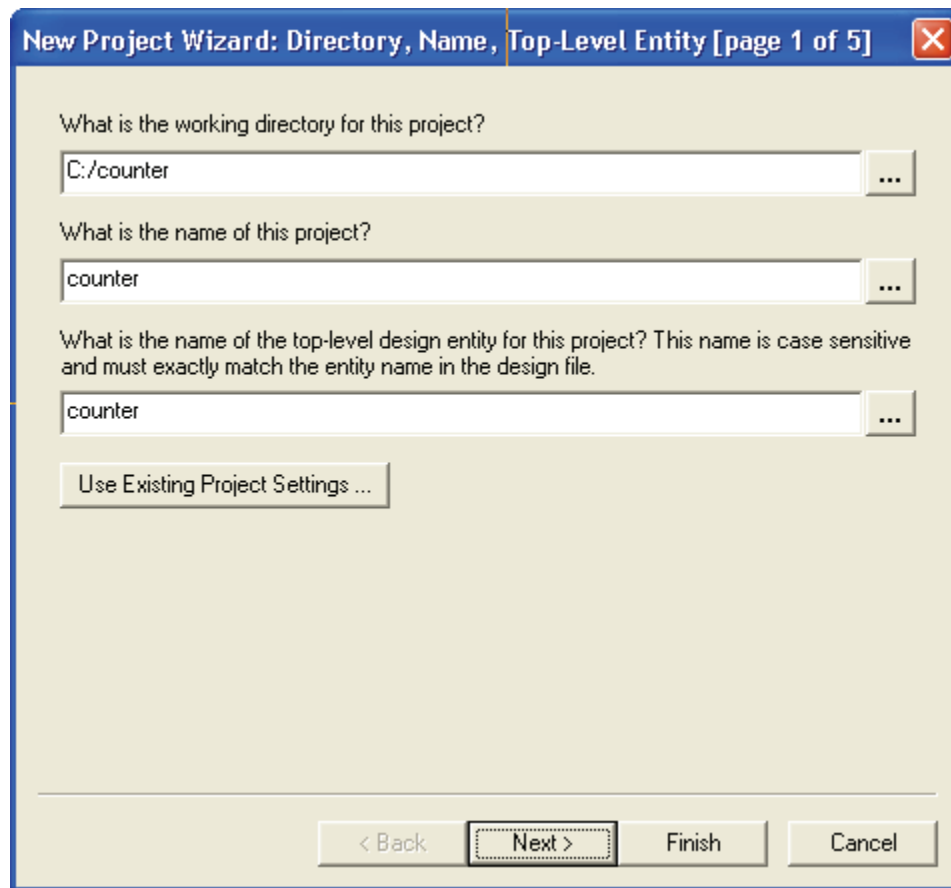


Figure B.2 The New Project Wizard: Directory, Name, Top-Level Entity window with the working directory, the project name, and the top-level entity name filled in.

2. Type in the directory for storing your project. You can also click on the  icon next to it to browse to the directory.
 - For this tutorial, browse to the directory `c:\counter` that you have created in Section B.1.1.
3. You also need to give the project a name.
 - For this tutorial, type in the project name `counter`.
4. A project may have more than one design file. Whether your project has one or more files, you need to specify which design file is the top-level design entity. The default name given is the same as the project name. However, you can use a different name.
 - For this tutorial, leave the top-level file name as `counter`, and click **Next** to continue to the next window.
 - Note that the file name and the module name (i.e., the name used in the HDL code for the module) must be the same.
5. In the New Project Wizard: Add Files [page 2 of 5] window, you can add the source files associated with your project.
 - For this tutorial, we want to add the source file `counter.v` (or `counter.vhd` if you are using VHDL) into the project. Since there is only one source file in the directory, we can simply click on the **Add All** button to add this one file into the project.

6. Click **Next** to continue to the next window.
7. In the New Project Wizard: Family & Device Settings [page 3 of 5] window shown in Figure B.3, we select the target PLD device that we will be implementing the circuit on. The UP2 board has two different PLD devices for programming: the FLEX 10K, which is the larger PLD, and the MAX7000S.
 - For this tutorial, we will use the FLEX 10K device. In the Family drop-down box, select **FLEX10K**.
 - In the Available devices list, select the device **EPF10K70RC240-4**. If this device is not listed, then you need to reinstall the Quartus II program, and make sure that all of the FLEX 10K devices are installed.
 - Click **Next** to continue to the next window.

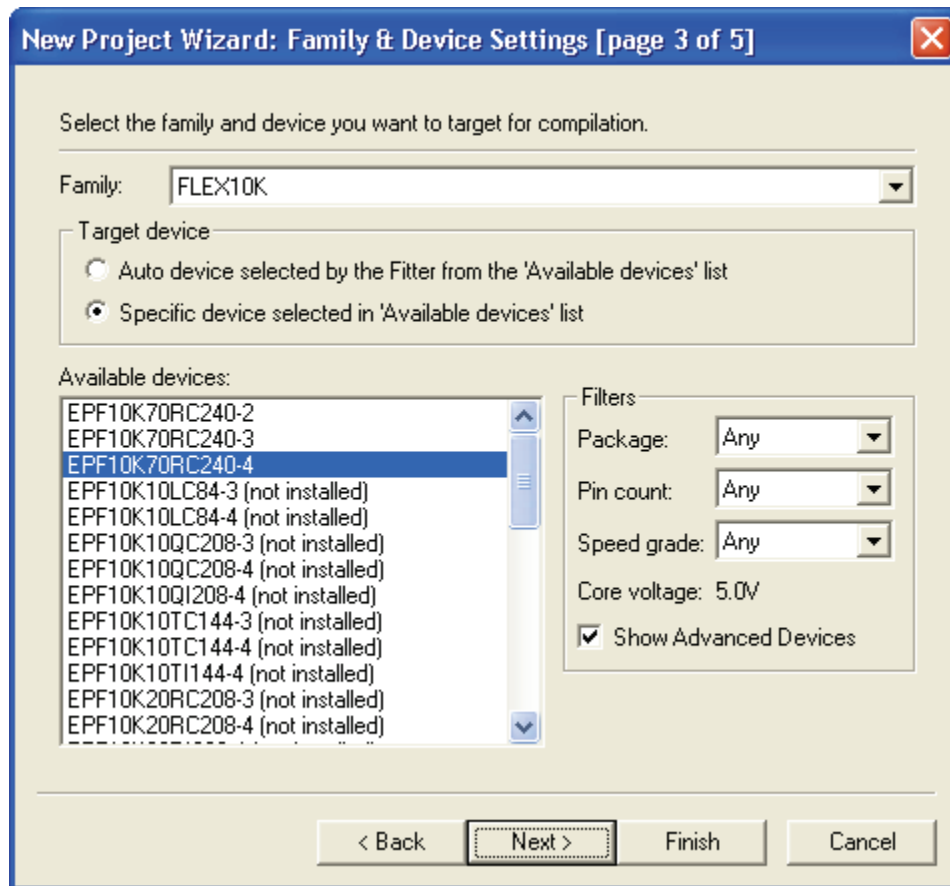


Figure B.3 The New Project Wizard: Family & Device Settings window with the device EPF10K70RC240-4 selected.

8. In the New Project Wizard: EDA Tool Settings [page 4 of 5] window, we do not have any EDA tools to use for this project, so click **Next** to continue to the next window.
9. The final window is a summary of the choices that you have just made. Click **Finish** to create your new project.

B.2 Managing Files in a Project

A project may have one or more design files associated with it.

B.2.1 Design Files in a Project

- To see the files that are currently associated with a project, click on the **Files** tab  in the Project

Navigator window as shown in Figure B.4. If the Project Navigator window is not displayed, then click on the Project Navigator button  to display it. Figure B.4 shows that this project has only one file named `counter.v`.

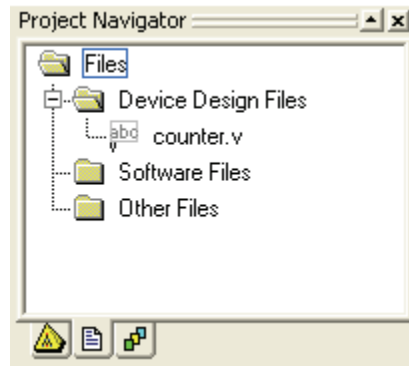


Figure B.4 Files associated with a project as shown in the Project Navigator window.

B.2.2 Opening a Design File

- To open a design file, simply double-click on the file that is listed in the Project Navigator window. Depending on the type of file, the associated editor will be used. The graphic editor is used to edit a Block Diagram/Schematic File, and a text editor is used to edit a VHDL or Verilog text file.
1. Double-click on the `counter.v` file to open it. The text editor is used to edit this source file. You can scroll through this file to see the Verilog code for describing the 4-bit binary counter. For this tutorial, we will not make any modifications, so you can close this file after viewing the code.

B.2.3 Creating a New Design File

- To create a new HDL design file, select **File | New** from the Quartus II menu. In the **Device Design Files** tab, select either **VHDL File** or **Verilog HDL File**. The newly created design file is not automatically added into the current project. If you want to include this new design file in the project, you have to add it in by following the instructions in Section B.2.4.

B.2.4 Adding Design Files to a Project

- To add another design file to the current project, select **Project | Add/Remove Files in Project** from the Quartus II menu. Alternatively, you can right-click on the folder icon labeled **Device Design Files** in the Project Navigator window, and then select **Add/Remove Files in Project** from the pop-up menu.
- This will bring up the Files window.
- From the Files window, you can choose additional files to be added into the project by either manually typing in the file name or browsing to the directory and then selecting it.
- Click on the **Add** button to add individual files, or click on the **Add All** button to add all of the files in the selected directory. For this tutorial, we do not need to add any new design files.

B.2.5 Deleting Design Files from a Project

- To delete a design file from a project, simply select it in the Project Navigator window, and then press the **Delete** key. Alternatively, you can right-click on the file that you want to delete, and then select **Remove File from Project**.

B.2.6 Setting the Top-Level Entity Design File

- In Section B.1.3 where it discusses how to create a new project, you also had to specify the name of the top-level design file. If you want to change the top-level entity to another design file, you can do so by right-clicking on the file that you want to be the top-level entity in the Project Navigator window. From the pop-up menu, select **Set as Top-Level Entity**.

B.2.7 Saving the Project

1. Select **File | Save Project** to save the project and all of its associated files.

B.3 Analysis and Synthesis

After describing your circuit with the Text Editor, the next step is to analyze and synthesize it. During this step, Quartus II collects all of the necessary information about your circuit, and produces a netlist for it.

1. From the Quartus II menu, select **Processing | Start | Start Analysis & Synthesis** to synthesize the circuit.

Alternatively, you can click on the icon .

2. If there are no errors in your circuit description, you should see the message “Quartus II Analysis & Synthesis was successful” in the Message window at the bottom.
3. If there are errors then they will be reported in the Message window and highlighted in red. You can double-click on the error message to see where the error is in the source file.

B.4 Circuit Simulation

Circuit simulation allows you to observe the behavior of the circuit before actually implementing the circuit in hardware. The Quartus II program can perform either a timing simulation or a functional simulation of a circuit. A functional simulation provides only information on the logic values of each signal simulated, whereas a timing simulation includes also the signal propagation delay information. In this tutorial, we will only perform a functional simulation.

B.4.1 Creating a New Vector Waveform File

To simulate a circuit design, you need to first create test vectors for specifying what the input values for your design are. Test vectors are specified in a vector waveform file having the file extension `.vwf`. In the vector waveform file, you will also specify what output signals you want to observe in the simulation.

1. From the Quartus II menu, select **File | New**.
2. Select the **Other Files** tab in the New window.
3. Select **Vector Waveform File** and click **OK**. A new Vector Waveform window similar to Figure B.5 opens up.
4. To change the time scale grid size increments to 5 ns, select **Edit | Grid Size**. Type in 5 for the time period, and select `ns` for the unit.
5. To overwrite the simulation input file with the simulation result, select **Tools | Options** to bring up the options window. Expand the **General** category if it is not already expanded by clicking on the plus sign icon. Select **Processing**, and put in a check mark in the check box for **Overwrite simulation input file with simulation results**. Click **OK** to accept the changes and close the window.
6. Select **File | Save** to save the Vector Waveform file. Use the default filename `counter.vwf`, which is the same as the top-level entity name but with the file extension `.vwf` (for vector waveform file). Make sure that the check box for **Add file to current project** is checked. The file will now be listed in the Project Navigator window under the folder **Other Files**.

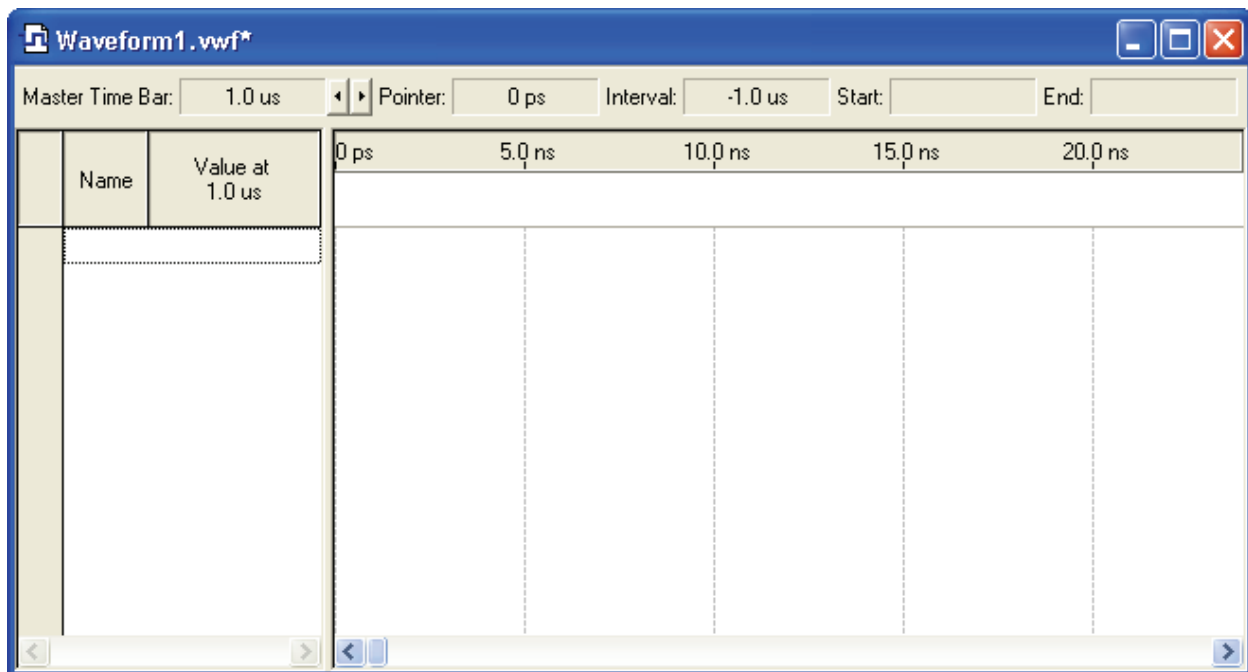


Figure B.5 A new Vector Waveform window for specifying the test vectors for simulation.

B.4.2 Selecting Input Test Signals

From the Vector Waveform window as shown in Figure B.5, you will select the test vectors to be simulated. Test vectors are the input and output signals from your circuit design.

1. From the Quartus II menu, select **Edit | Insert Node or Bus**. Alternatively, you can double-click on the white area below the heading label **Name** in the Vector Waveform window.
2. In the Insert Node or Bus window, click on the **Node Finder** button to bring up the Node Finder window.
3. Make sure that the **Filter** selected is **Pins: all**. Click on the **List** button to list all of the available pins from your circuit design in the Nodes Found (left side) pane as shown in Figure B.6.
4. Select the signal(s) that you want to see in the simulation from the Nodes Found pane, and then click on the **>** button to move the selected signal(s) to the Selected Nodes pane. You can hold down the **Ctrl** key to select multiple signals. Clicking on the **>>** button will move all the signals listed in the Nodes Found pane to the Selected Nodes pane.
 - For this tutorial, select the two input signals `Clear` and `Clock`, and the two output signals `Overflow` and `Q`. Note that for the bus signal `Q`, you need to select the entire bus and not the individual bits of the bus (such as `Q[0]`).
 - The symbols  and  next to the signal names denote whether the signal is an input or output signal respectively.
5. Repeat Step 4 until you have selected all of the signals that you want to see in the simulation.

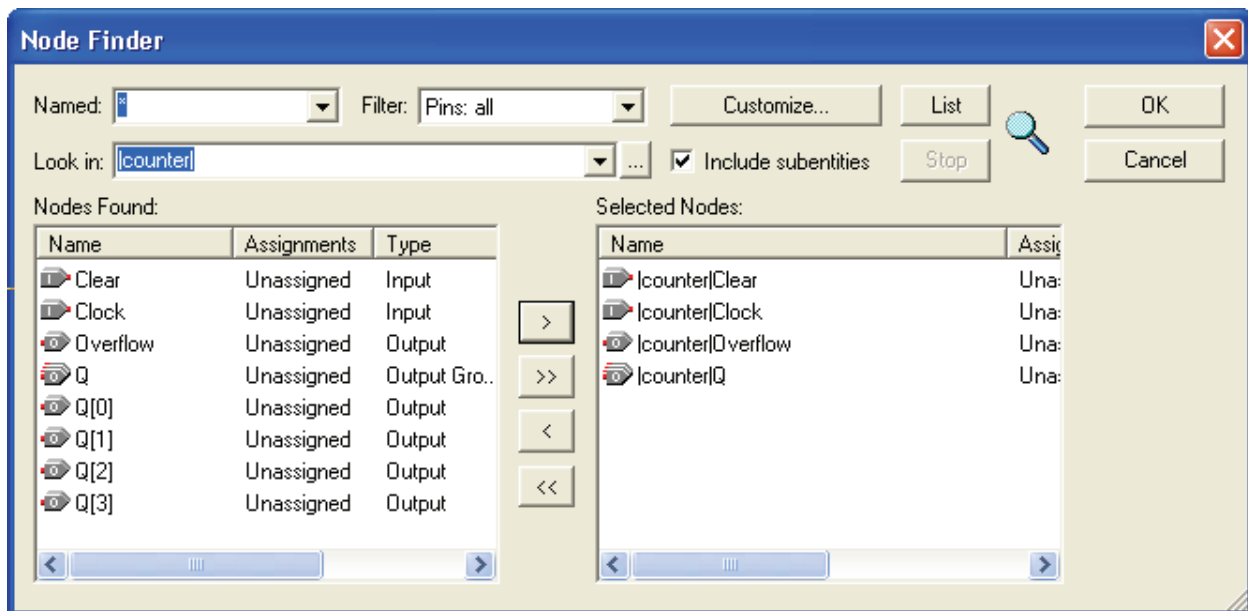


Figure B.6 The Node Finder window for adding input and output signals for simulation.

- Click on **OK** when you are finished. The four selected signals will now be transferred to the Insert Node or Bus window having the generic name “Multiple Items.”
- Click on the **OK** button in the Insert Node or Bus window to insert the selected signals to the Vector Waveform window as shown in Figure B.7.

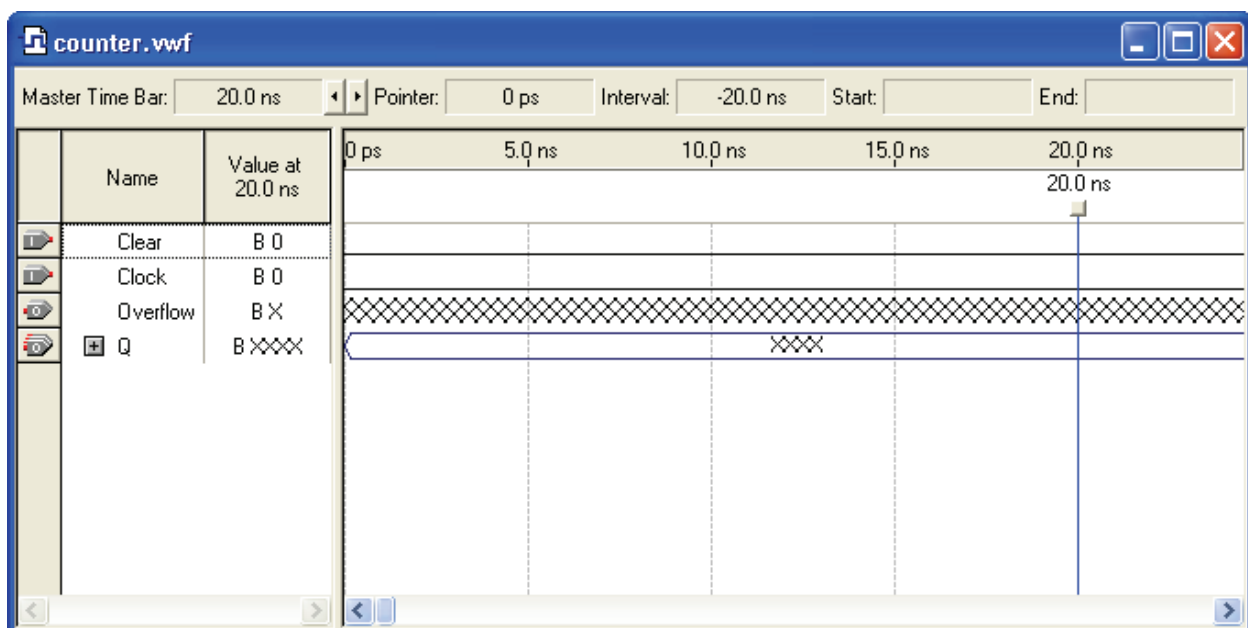


Figure B.7 The Vector Waveform window with the four signals for simulation.

B.4.3 Customizing the Vector Waveform Window

- You can rearrange the signals in the Vector Waveform window by dragging the signal icons such as  up or down. First select the signal by clicking on the  icon that you want to move. Then drag it to the new location.

1. For this tutorial, move the signal `Clock` from where it is to be the first signal listed as shown in Figure B.8.
 2. Move the signal `Overflow` to the end.
- To delete a signal, just select the signal by clicking on its name and then pressing the **Delete** key.
 - For bus signals, you can see the individual bits by clicking on the plus icon to expand it.
 - To change the radix of the displayed value, right-click on the signal name and select Properties. In the Node Properties window, change the Radix to what you want.
1. For this tutorial, change the radix for the bus signal `Q`, to be Unsigned Decimal.

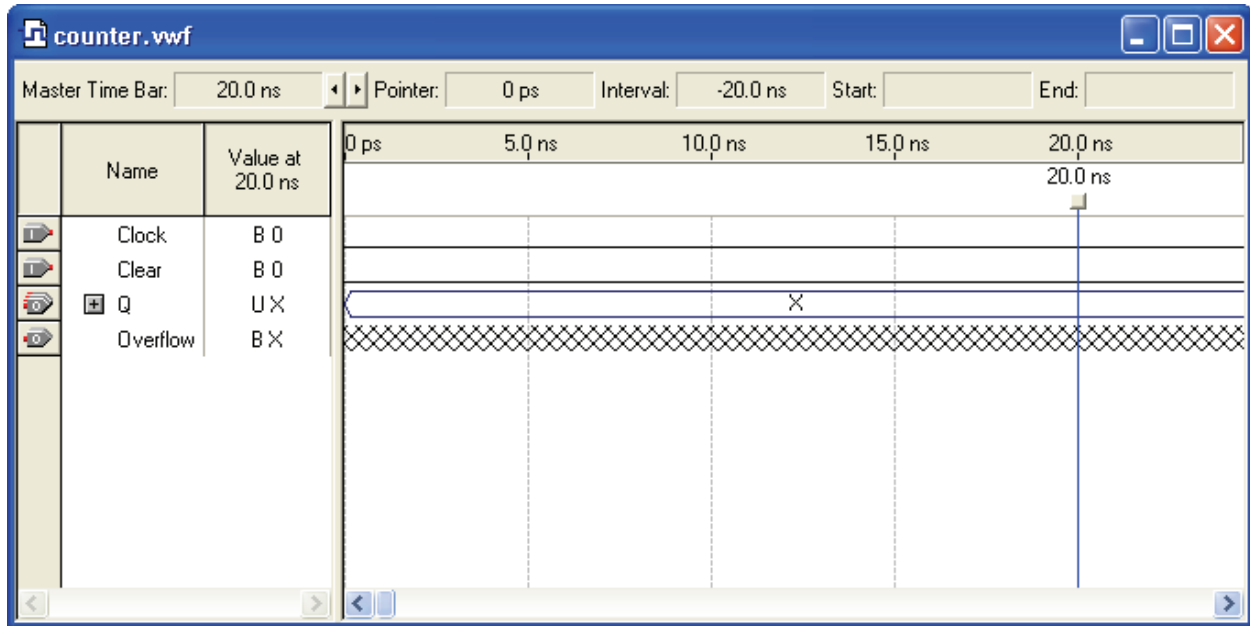


Figure B.8 The Vector Waveform window after rearranging the signals.

B.4.4 Assigning Values to the Input Signals

The next thing is to assign values to all of the input signals.

1. Using the Selection pointer tool, select the `Clock` signal by clicking on the signal name.
2. Click on the **Clock** icon  in the toolbar on the left to define the `Clock` signal. Leave the time period at 5.0 ns. Click **OK**, and observe the changes made to the `Clock` signal as shown in Figure B.9.
3. Using the Selection pointer tool, drag from time 0 ps to 10 ns for the `Clear` signal only. While dragging the mouse, the selected signal range will be boxed in, and when you release the mouse the selected area will be highlighted in blue.
4. Click on the **Forcing High** icon  in the toolbar on the left to set the signal in the selected range to a logical 1 value.
5. Select **File | Save** to save the vector waveform file. The filename should be `counter.vwf`.

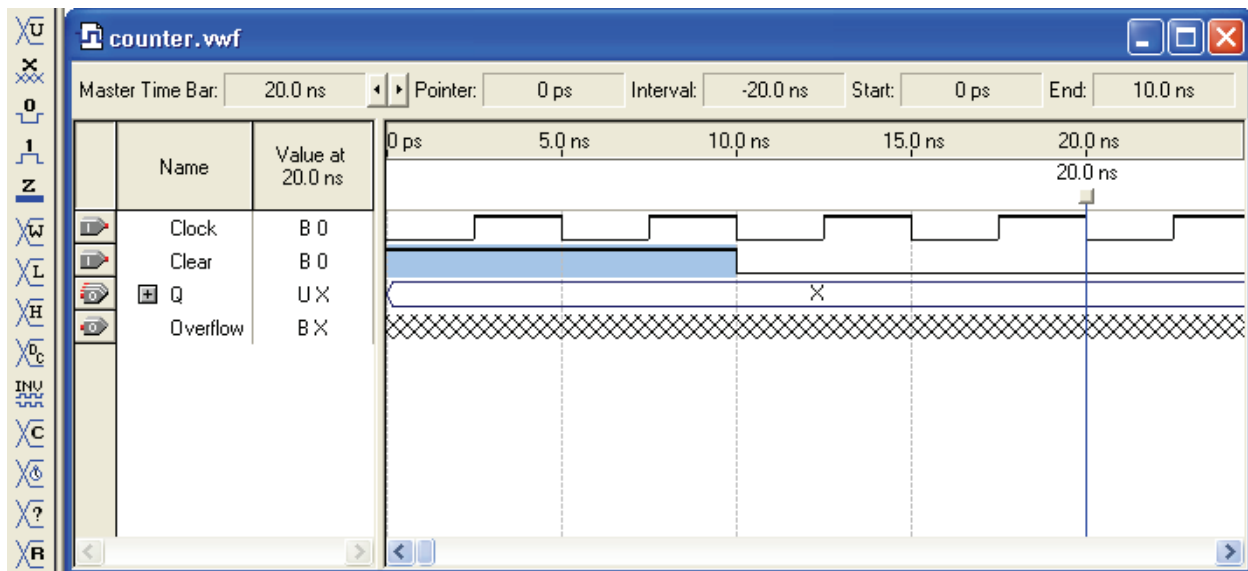


Figure B.9 Changing the input signal values.

B.4.5 Generate Functional Simulation Netlist

In order for the Quartus II program to perform a functional simulation of the circuit, it must first generate a functional simulation netlist of the circuit.

1. From the Quartus II menu, select **Tools | Simulator Tool** to bring up the Simulator Tool window as shown in Figure B.10.
2. In the Simulator Tool window, make sure that the Simulation Input filename is `counter.vwf`.
3. From the **Simulation mode** drop-down menu, select **Functional**.
4. Click on the **Generate Functional Simulation Netlist** button.
5. If there are no errors in your circuit, you should see the message "Quartus II Analysis & Synthesis was successful" in the Message window at the bottom.
6. If there are errors then they will be reported in the Message window and highlighted in red. You can double-click on the error message to see where the error is in the source file.

B.4.6 Starting the Simulator

We are now ready to simulate the design.

1. In the Simulator Tool window as shown in Figure B.10, put a check mark in the box that says **Overwrite simulation input file with simulation results**.
2. Click on the **Start** button  and watch the progress of the simulation.
3. At the completion of the simulation, you should see in the Message window at the bottom, a line that says the simulation was successful.

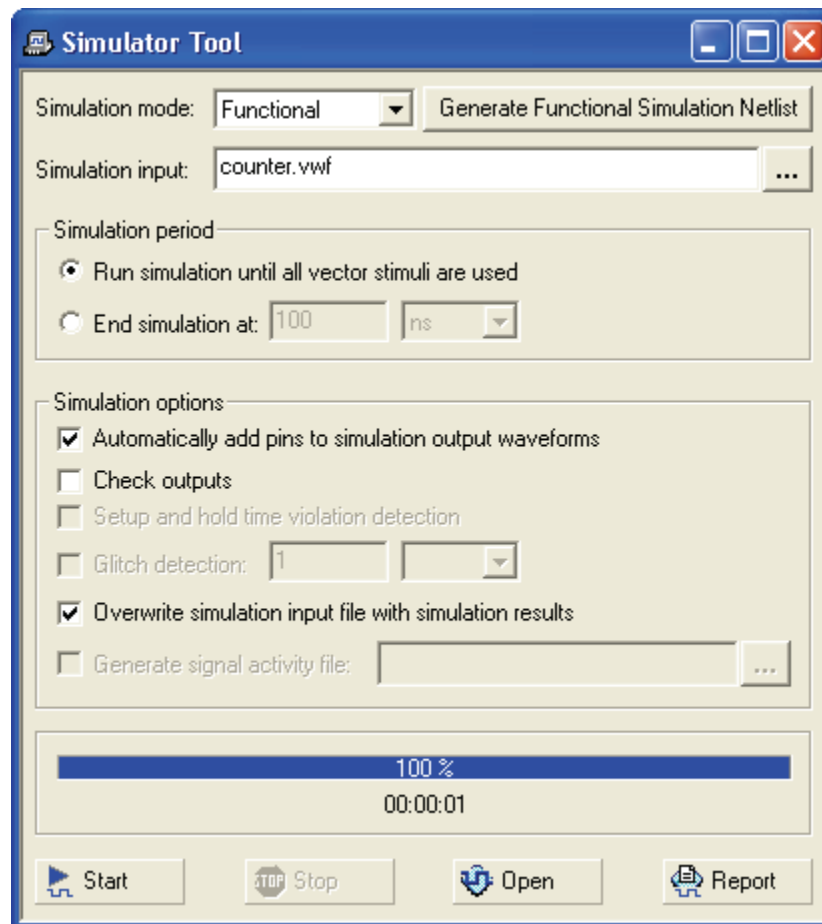


Figure B.10 Simulator Tool window.

B.4.7 Viewing the Simulation Results

1. To see the result of the simulation, you can either select the Vector Waveform window `counter.vwf`, or click on the **Open** button.
2. If a message window appears asking whether you want to reload the vector waveform file to update the changes made by the simulator. Click **Yes**.
3. The resulting waveform from the simulation is shown in Figure B.11.
4. Click on the Zoom Tool icon  in the toolbar on the left to zoom out so that you can see one complete cycle of the count inside the window. With the mouse placed somewhere inside the waveform area (the mouse pointer changes to a crosshair with a magnifying glass), hold down the **Shift** key while you click on the mouse to zoom out. Click several times until you can see a full cycle of the 4-bit count (i.e., from 0 to 15) inside the window. Notice that the count signal `Q` starts counting at the first rising edge of the clock after the `Clear` signal is deasserted. Furthermore, when `Q` reaches 15, the `Overflow` output is set to a 1.
5. You can change the `Clear` input signal to something different to see what happens to the `Q` output. After making any changes to the simulation file, you need to simulate the design again by clicking on the Start button . However, it is not necessary to re-generate the functional simulation netlist.

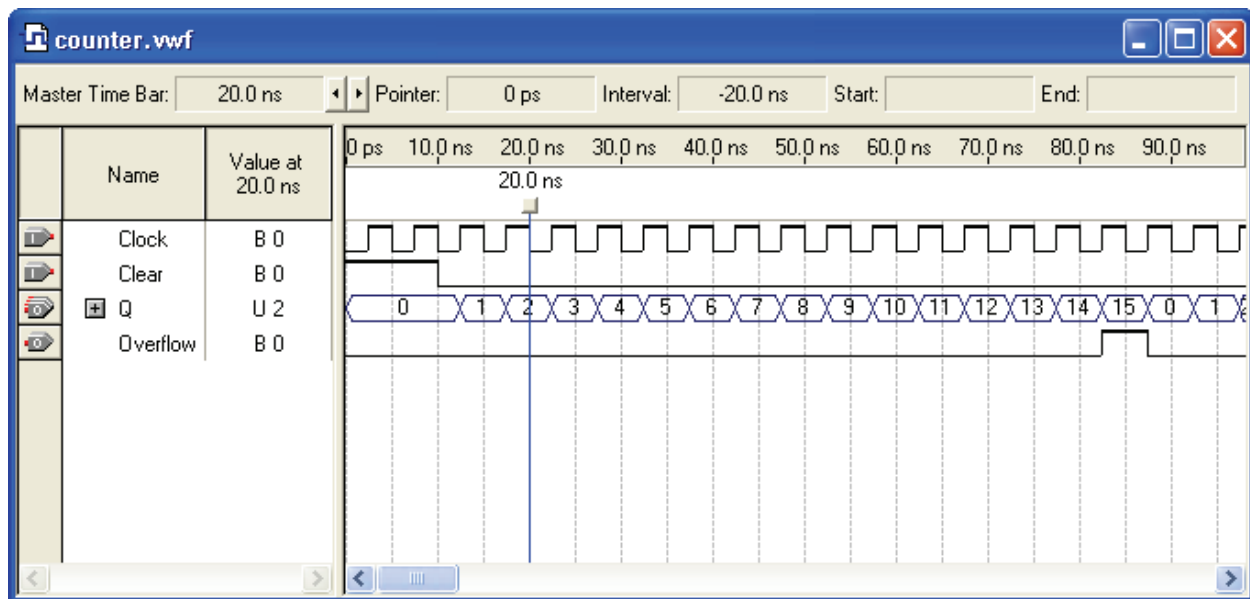


Figure B.11 Resulting waveform after the simulation.

B.5 Creating and Using a Logic Symbol

If you want to use this circuit as part of another circuit in a schematic drawing, you can create a logic symbol for this circuit. However, this is not necessary if you use this circuit in another Verilog or VHDL design file.

1. To create a logic symbol, first select the Text Editor window `counter.v` as the active window.
2. Select **File | Create/Update | Create Symbol Files for Current File**. The name of this logic symbol will be the same as the name of the current active HDL file (`counter`) in the Text Editor, but with the file extension `.bsf` (for block symbol file).
3. You can view and edit the logic symbol by first opening the file. Select **File | Open** and type in the filename `counter.bsf`. Click on the **Open** button. A window similar to Figure B.12 will open showing the logic symbol.

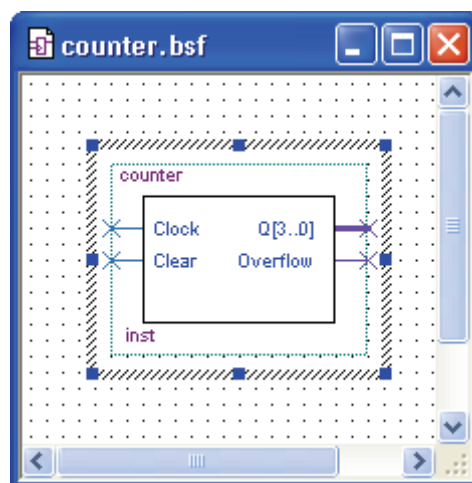


Figure B.12 Logic symbol of the counter circuit.

4. The placements of the input and output signals can be moved to different locations by dragging the signal

connection line around the symbol box. The signal label will also be moved. You can then drag the label to another location if you wish.

5. The size of the symbol can also be changed by dragging the edges of the symbol box.
6. This new symbol name can now be used in the Graphic Editor. It will show up in the Symbol window under the `Project` folder. You can follow the same steps as discussed in Tutorial 1, Section **Error! Reference source not found.**, to insert this logic symbol into another schematic circuit design.
7. To use the counter circuit that is represented by this logic symbol in another project, you need to first copy the `counter.bsf` symbol file and the corresponding `counter.v` HDL design file to the other project's directory.