Department of Electrical and Computer Engineering

COEN 6501 Dec. 8, 2014

Answer all Questions. All Questions carry equal marks

Exam Duration 3 hour

No books, papers are allowed. Lecturer: Asim J. Al-Khalili

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Question 1

1. Implement F using 2:1 MUXs only. All inputs should be of non-inverting type.

F = ABC’ + AB’C’ + ABC+ A’B’C

1. Implement the same functions using look up tables.

**Note:** You are allowed to minimize F.

Question 2

Design a hardware using carry save adder arrays to calculate y.
**y= N2 + N +1**N is an unsigned binary number 4 >N>0. Evaluate your design in terms of speed and area

**Question 3**

Design a shift and add multiplier controller as shown in Fig.1. The controller has two inputs:

 **L**: the least significant bit of the multiplier operand, “0” or”1”

**N**: Counter output “0” or”1”

The controller has one output.  **S**: Stop signal “0” or”1”

Operation of the controller is as follows:

The controller is usually in the idle state.

 If L is ‘1’, then an add and shift operation is performed, If LSB is ‘0’ then a shift operation is performed. In both cases, the counter counts up by one step.

When the counter reaches it desired value N=1, a ***Stop*** signal **S=1** is generated and the state machine goes to the stop state. Design the **sequential circuit *starting with a state diagram***

**Note:** The counter and the reset mechanism are designed separately.

**Shift and Add**

L

N

**S**

 **Fig.1**

**Question 4**

**a.** Identify all the paths in the circuit shown in the Fig. 2 below.

**b.** Determine maximum speed of operation at typical conditions for the

Timing parameters for all components are listed in Table 1.

**c.** At the maximum speed of operation, determine the slack time for the setup time and hold time at the D-input of Flip-Flop U2.

 D

D Q

 Q

D Q

Z

CLK

U2

U5

U6

U7

U8

U9

U10

U11

U3

U1

U4

 **Fig. 2**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Component | Tp (ns) | Input Loading (UL) | K1**ns/UL** | K2 ns/fanout |
| Inverter | 0.15 | 1 | 0.1 | 0.08 |
| NAND/NOR(2input) | 0.24 | 2 | 0.05 | 0.14 |
| NAND (3 input) | 0.4 | 1.5 | 0.12 | 0.18 |
| Flip Flop, ↑, (CK to Q) **Tsu=1 ns, th = 0.5ns**  | 1.5 | 2 | 0.1 | 0.2 |

**Table 1**

**Question 5**

a. The Circuit shown in Fig. 2 operates at a frequency 50 MHz. Signal A arrives at -∞. Determine the arrival time, the required time and the slack time at points B and C.

b. Determine the maximum clock frequency, considering worst case scenario.

 The circuit is implemented on a die, packaged in a ceramic DIP with a thermal resis­tance of 30oC/W. Power consumption of the chip is 1.5 W with room temp at 25C. Fanout loading is neglected. Use Table 2 parameters.

c. Determine the maximum frequency of operation if skew is **−2ns.**

**D1 Q**

**D2 Q**

Q

Q

**D1 Q**

**D1 Q**

**CLK**

**D2 Q**

CLKd

**D2 Q**

**CLK**

D2

**D3 Q**

0.2ns

0.4ns

0.3ns

U3

U1

U2

A

**B**

 **C**

|  |  |  |  |
| --- | --- | --- | --- |
| Component | Tp (ns) | Input Loading (UL) | K1ns/UL |
|  AND/(2input) | 0.2 | 1 | 0.15 |
| OR (2 input) | 0.3 | 2 | 0.25 |
| XOR (3 input) | 0.4 | 3 | 0.35 |
| Flip Flop, ↑, (CLK to Q) **Tsu=1 ns, th = 0.5ns , tskew=2ns** | 2 | 4 | 0.45 |

 **Fig. 2**

 , K’ = KT \* KV \*K KT = , TJ = Tamb + Φ Ja \* PdKV =  , KP = 1+ 0.01 \* fP

 **Table 2**

**Question 6**

For the circuit shown below,

1. Write a structural VHDL code for the entity “Adder”.
2. Write behavioral VHDL code, “Test\_Bench” for testing the circuit

Test\_Bench

Adder

Generator



1. Draw a response to the following VHDL Code

 ***process***

 ***begin***

 B<= ***not*** A ;

 ***wait until*** A=‘1’ ***for*** 10 ns;

 ***end process***;

 A

 10 20 30 40 50 60

 B -------------------------------------------------------------?

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**Appendix A**

**1. tcs,max < tCQmin + tCLmin + tsu.min**

**2. Tmin ≥ tCQmax + tCLmax+ tsUmaxR2 –tcsmin**

**3. thmaxR2 < tCQmin + tCLmin - tcsmax**

**tCL = tLogic + tinterconnec**