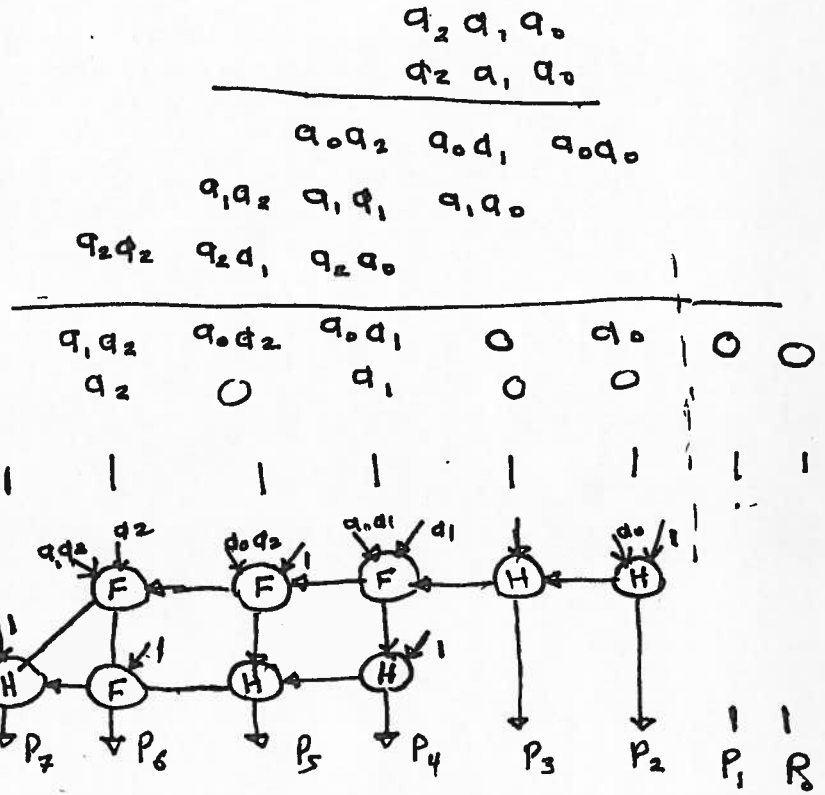


Q1

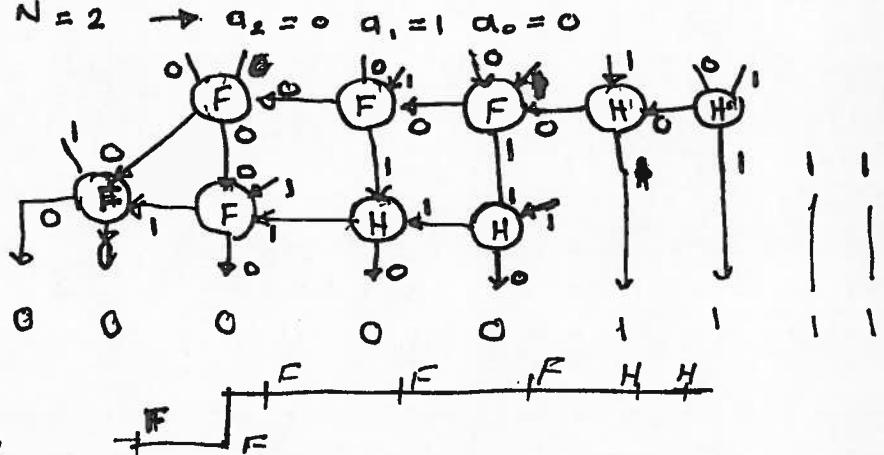
$H(N(N)-1) \quad N = a_2 a_1 a_0$



Shift 2 places to left

add -1

Implementing the architecture with $N=2 \rightarrow a_2=0, a_1=1, a_0=0$



$H(2(2))-1 = 15$

Delay = $2\tau_H + 5\tau_F + \tau_{AND}$

Area = $4A_H + 5A_F + 9A_A$

Q 2

7th Sem Fall 2016

We design an optimum carry select adder & carry ripple adder, determine their delay and area. Multiply delay and area for each case and then select the AT.

- Carry Ripple Adder

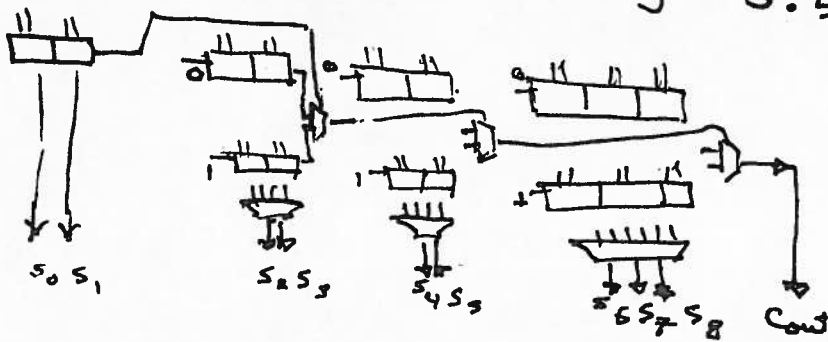


$A_{CRA} = 9 A_{FA}$ Delay = $9 \tau_{FA}$

- To calculate the best carry select adder we see the best combination that gives the minimum delay as the area is almost constant.

- | | | | |
|-----------|------------------------|-------------|---------------------------------------|
| 3 3 3 | 4 τ_F | 1 1 1 2 2 2 | 3 $\frac{1}{2} \tau_{FA}$ Area = 17.3 |
| 4 5 | 5 $\frac{1}{2} \tau_F$ | | |
| 5 4 | 5 $\frac{1}{2} \tau_F$ | | |
| 3 2 2 2 | 4 $\frac{1}{2}$ | | |
| ✓ 2 2 2 3 | 3 $\frac{1}{2}$ ✓ | | |

Delay = $3.5 \tau_{FA}$



Area of Design = $16 FA + 10 MUX = 16 + \frac{10}{3} = 19.3 A_{FA}$

AT of Carry Ripple Adder = $9 * 9 = 81 \tau_{area}$

AT of Carry Select Adder = $3.5 * 19.3 = 67.55 \tau_{area}$

Therefore The carry select adder is the best design

Q3

Using IEEE 754 Format

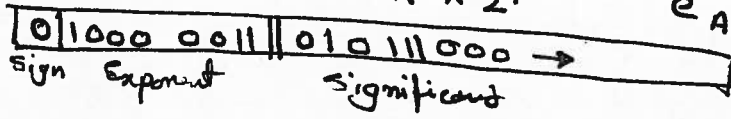
bias is $E = e - 1 = 127$

$A = 21.75 = 10101.11$ or 1.010111×2^4

Signbit $S = S_A \oplus S_B$

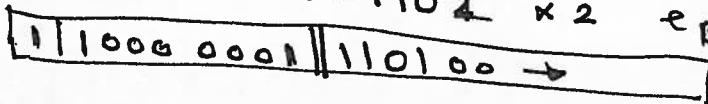
$e_A = 4$

Packed form of A



$B = -7.25 = 111.01 = -1.1101 \times 2^2$

B



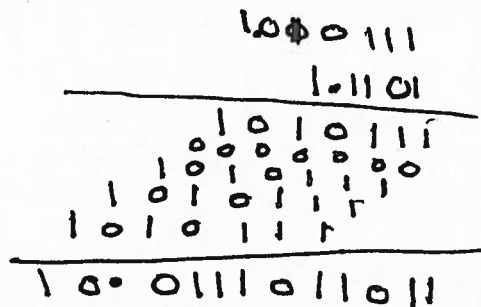
$e_B = 2$

* $\rightarrow S_R = 1 \oplus 0 = 1$

$\rightarrow E_R = 10000011 + 10000001 - 01111111$
 $= 10000100 + 10000001 \leftarrow 2's \text{ Complement of } 01111111$
 $= 10000101 = (133)_{10}$

$S_R = 1.010111 \times 1.1101$

$Sig_R = 10.0111011011$



Adjusting exponent & Significant

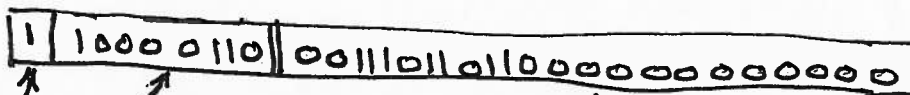
* $E_R = 10000101 + 00000001 = 10000110$

$Sig_R = 1.00111011011000$

Rounding the results

* $Sig_R = 1.0011101101100$

Packing the result



Sign of Result

Exponent of Result

Significant of result