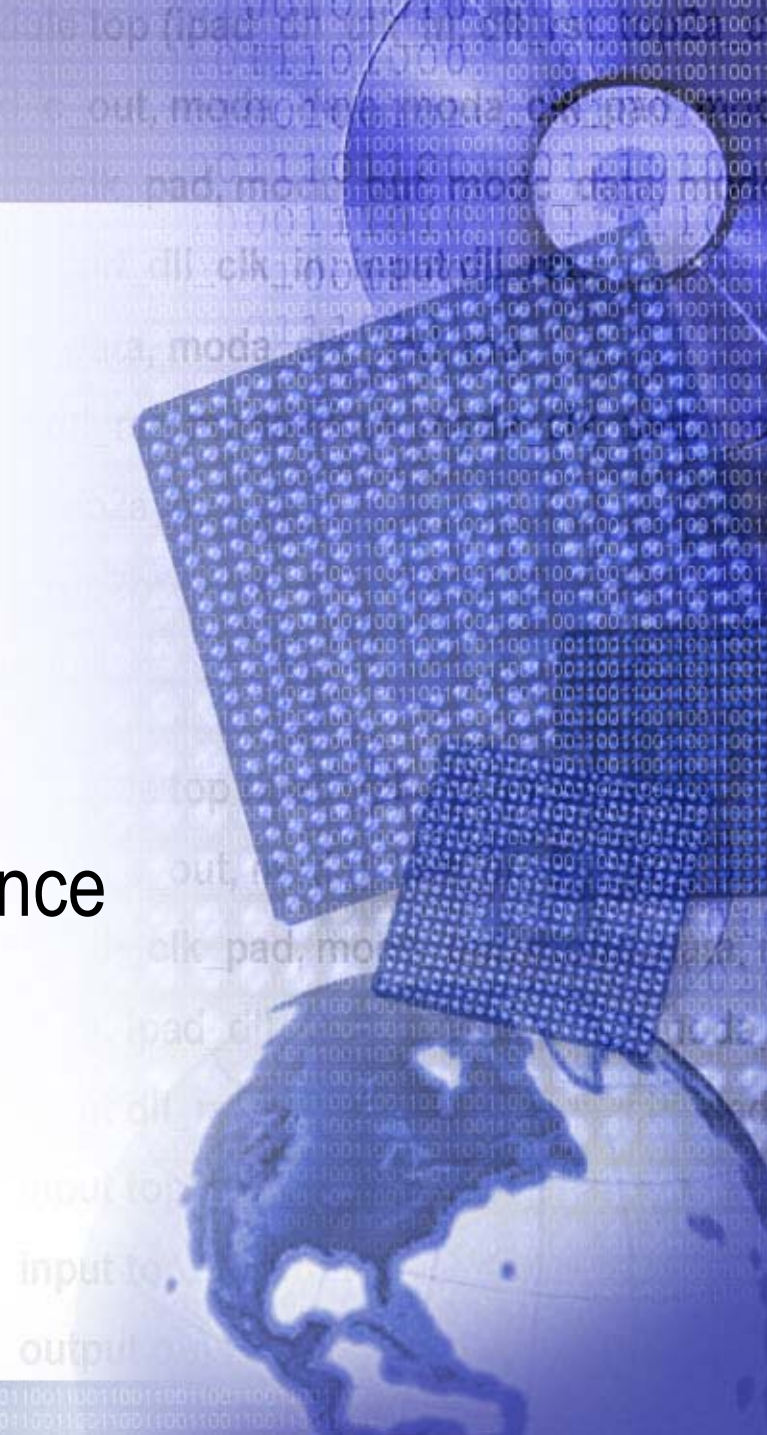




Virtex™-4 Performance Advantage

Achieving Breakthrough Performance
with the World's Fastest FPGA



A red, jagged-edged badge with the text "500 MHz" in white, slanted upwards to the right.

500 MHz

500 MHz Virtex-4...

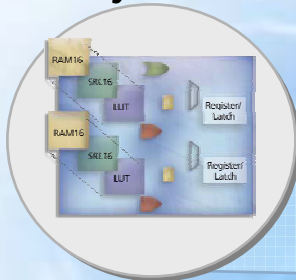
1. 90 nm **technology** is the foundation
 - More transistors, faster speed and lower cost
2. Clever **circuit design** builds on that foundation
 - Smaller size, lower power, and higher performance
3. **Architectural innovation**, novel features
 - Hard-coded IP:
 - PowerPC®, BRAM-FIFO, DSP-MAC
 - Source-synchronous I/O with delay-line on every pin,
 - Dedicated Multi-Gigabit Transceivers up to 10 Gbps
4. Continuously improving design tools, easier to use

...the fastest FPGA family in the world



Architectural Innovation

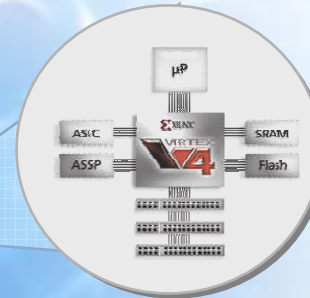
**500 MHz
Logic Array**



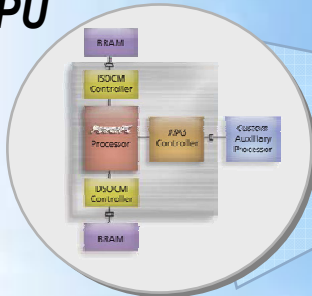
**500 MHz
Differential
Clocking**



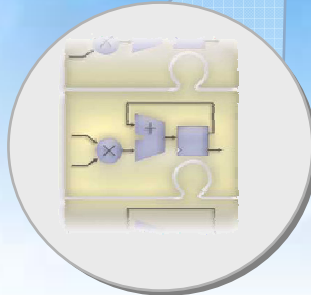
**>1 Gbps diff I/O
with ChipSync™**



**450 MHz PowerPC
with APU**



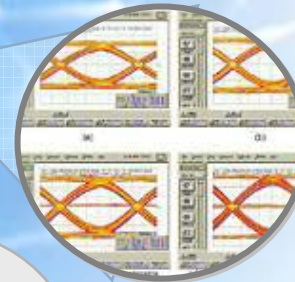
**500 MHz
XtremeDSP
Slice**



**500 MHz
BRAM and FIFO**



**622 Mbps to over 10 Gbps
RocketIO**



Better Functions = Higher Speed

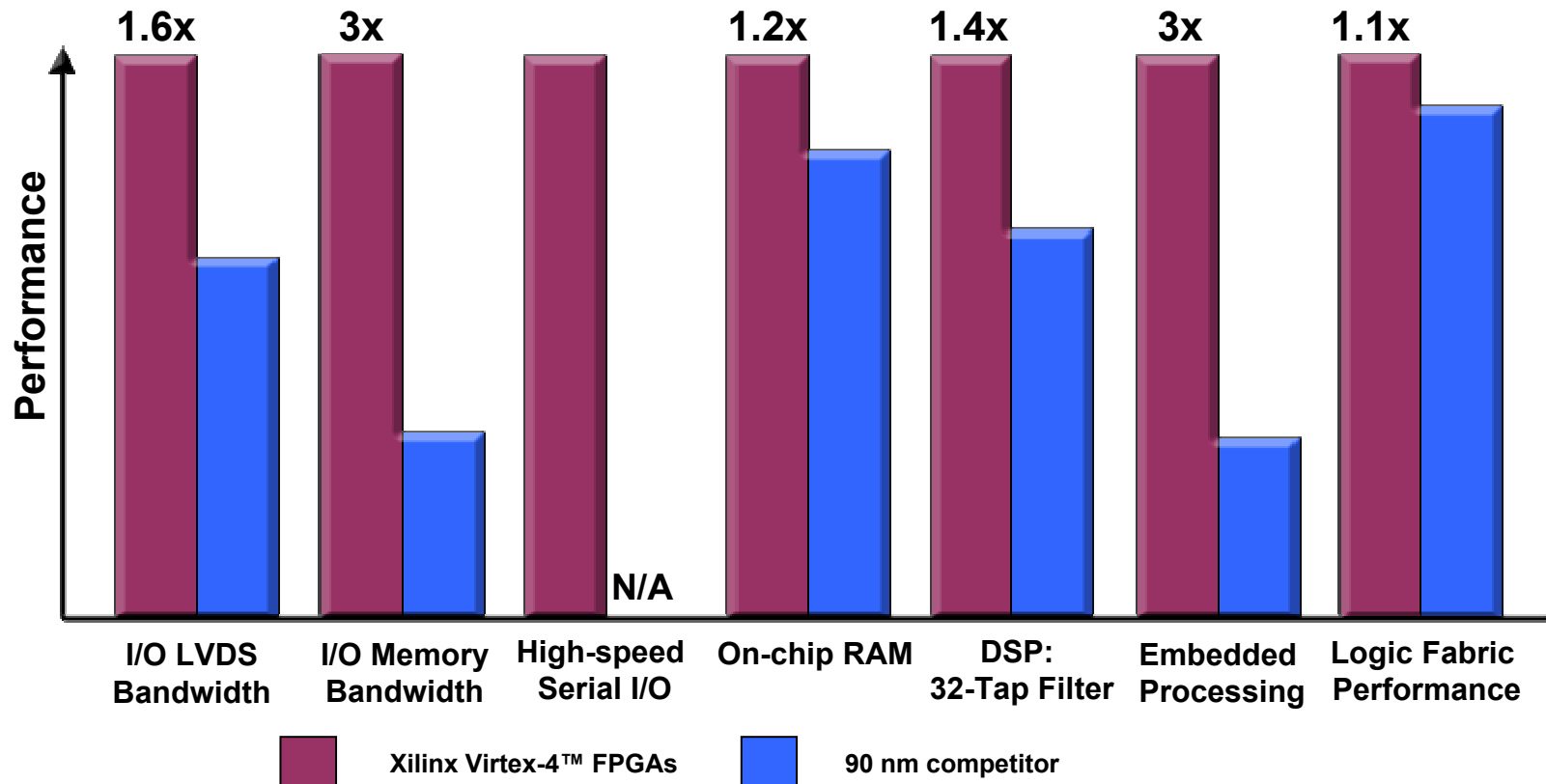
The biggest performance boost comes from:

- Versatile clocking
- Parallel I/O and memory interfaces
- Serial I/O, multi-gigabit transceivers
- Memory (distributed RAM, BlockRAM, FIFOs)
- Expandable DSP slices
- Fast synchronous counters
- Embedded processing
- Fabric logic resources and interconnect structure

Functionality can triple the performance



Virtex-4 Leads in 7 of 7 Performance Criteria

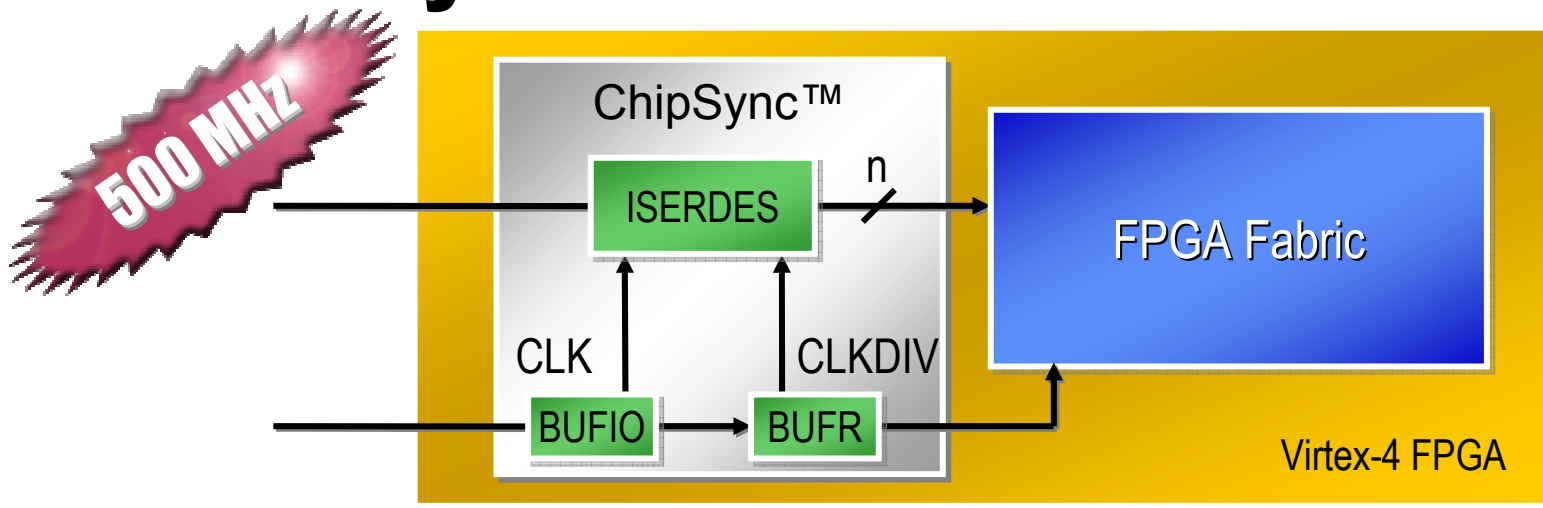


Data based on competitor's published datasheet numbers

Performance up to 3x higher than competing FPGAs



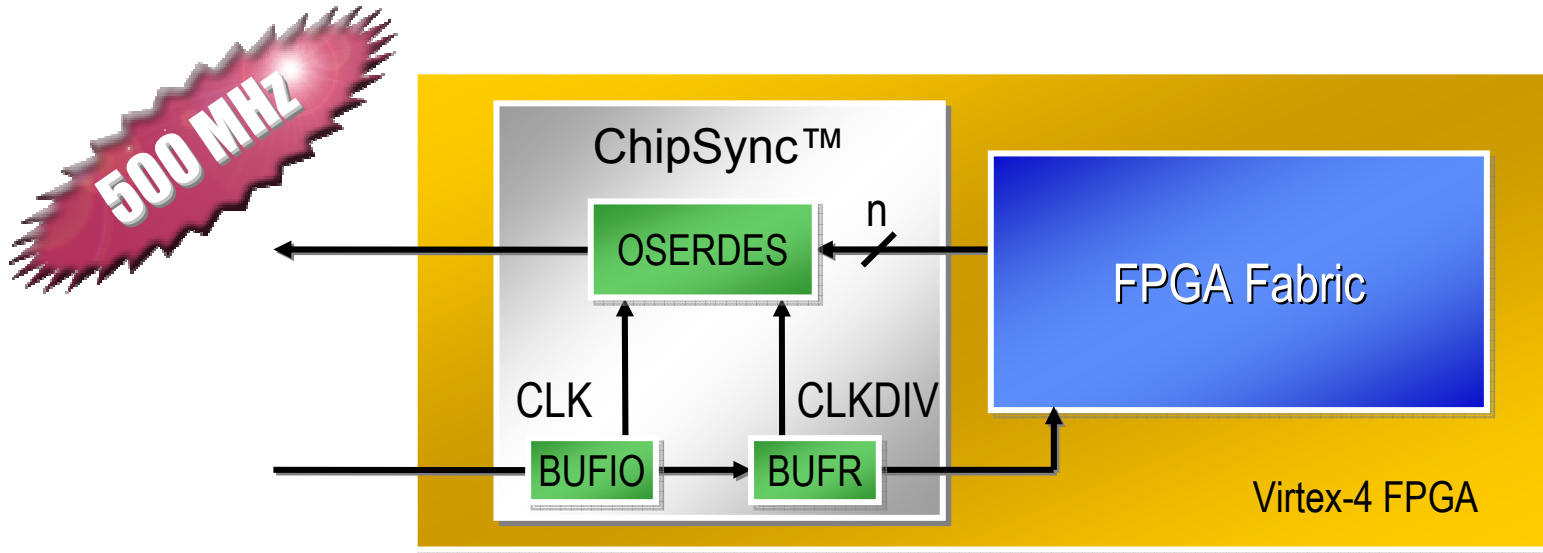
Built-in Support for Source-Synchronous Interfaces



- Serial-to-Parallel Converter on every input pin
 - Frequency division by 2, 3, 4, 5, 6, 7, 8 or 10
- Works in conjunction with IDELAY block
 - Dynamic signal alignment for bit, word, or clock
 - Supports Dynamic Phase Alignment (DPA)

Requires no resources in the fabric

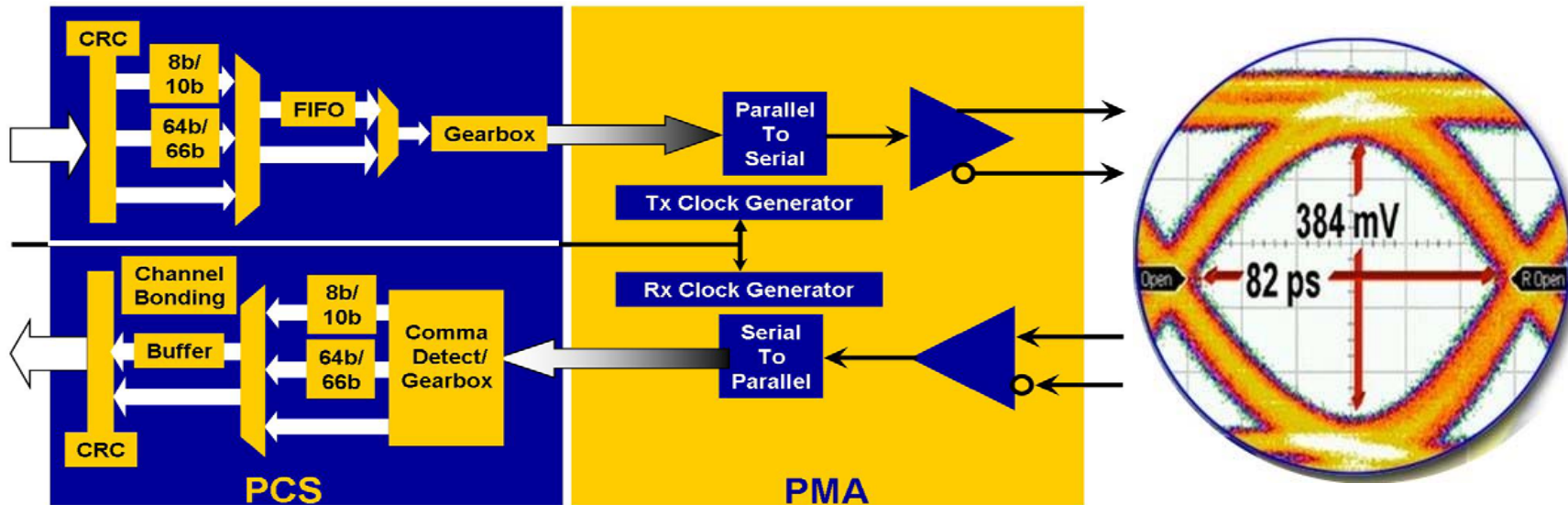
Built-in Support for Source-Synchronous Interfaces



- Parallel-to-Serial Converter on every output pin
 - Frequency multiplication by 2, 3, 4, 5, 6, 7, 8 or 10

Requires no resources in the fabric

Fastest Serial I/O



- **RocketIO™ transceivers**

- Full-duplex w/ integrated SERDES, FIFOs, and CDR
- 8-24 channels per chip, Data rate: 622Mbps-10Gbps
- Transmit pre-emphasis, receive equalization

Fastest I/O in any FPGA

DSP Building Block

- FPGAs do high-performance DSP extremely well
 - Thanks to massive parallelism (500+ engines)
 - Fast clock rate, pipelined, high throughput
- Needs many fast Multiplier-Accumulators (MACs)
 - Dedicated, repetitive (systolic) structure
 - Slightly programmable, must be expandable

Build the fastest DSP implementations



Unbeatable DSP Performance

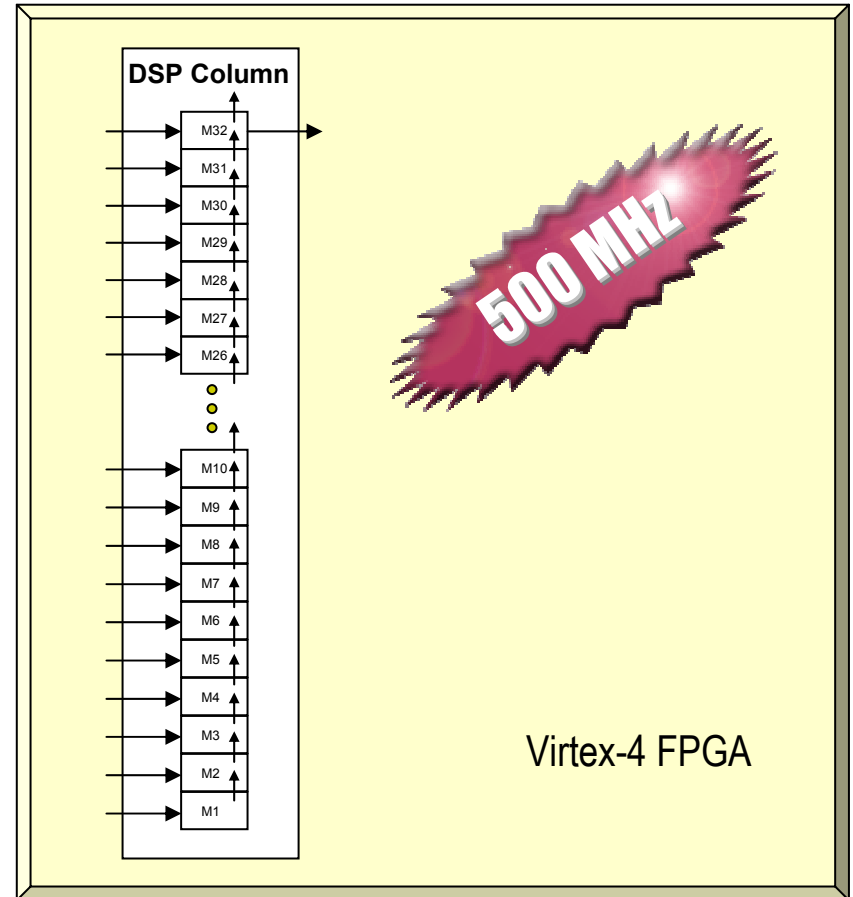
ASMBL advantage:

- Cascade throughout vertical column without any help from the fabric
- Speed not affected by external adder tree
- 57% faster than the traditional approach

Example:

Systolic 32-tap FIR Filter

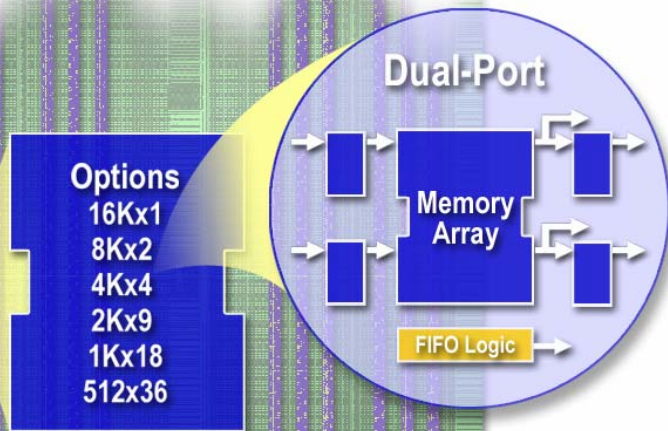
- 400 MHz in Slow grade
- 500 MHz in Fast grade



It helps to do things right!

500 MHz

Fast 18Kb-BlockRAM



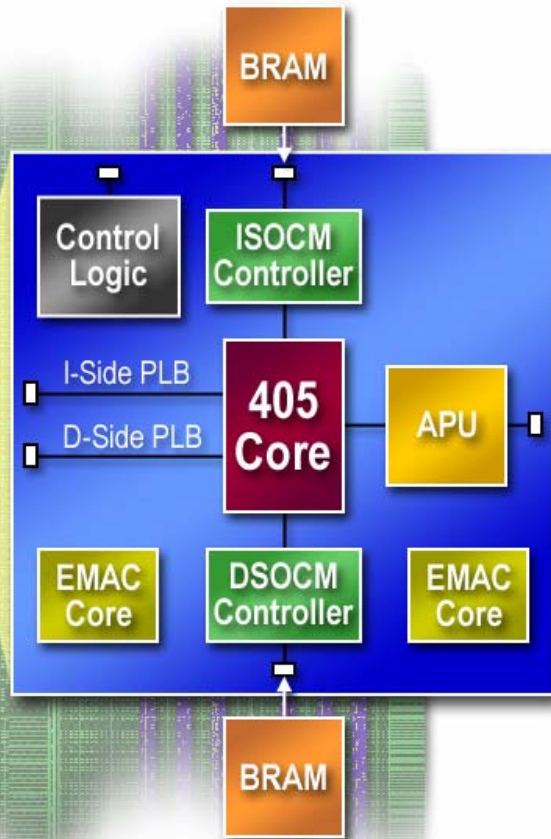
- Pipelined 500MHz synchronous operation
- Width-adjustable per port
- Read before write, or write before read
- Built-in FIFO controller in each BlockRAM
- Built-in Hamming error correction for 64 bits

Ideal for

- Microprocessor data / instructions and fast state machines

48 to 552 BlockRAM per chip

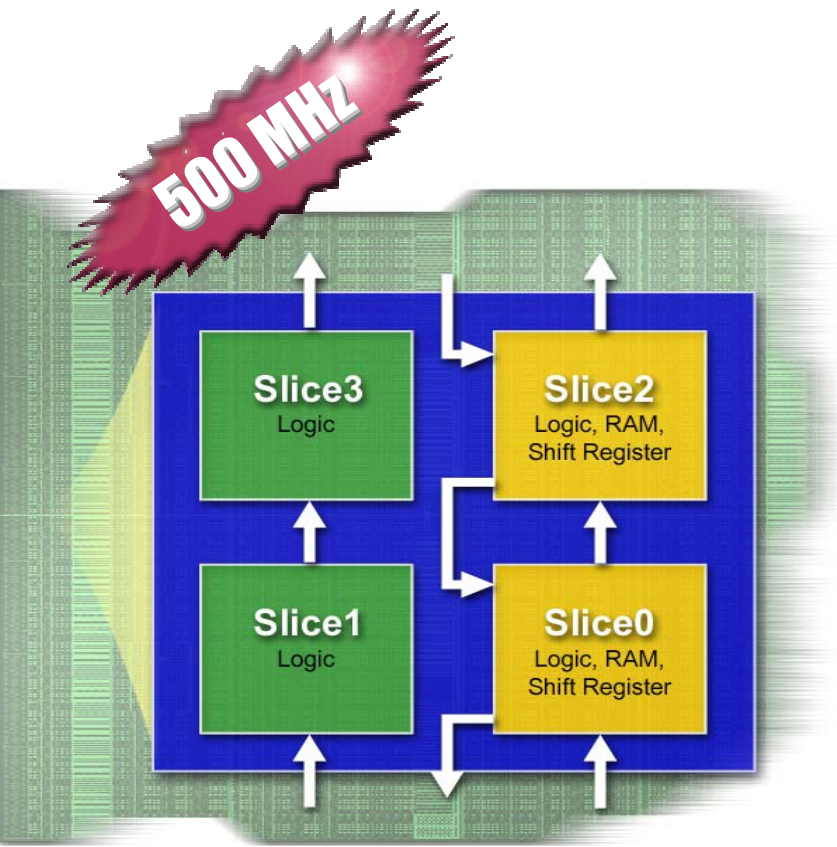
Highest-Performance FPGA Microprocessor



- **High-performance PowerPC Core**
 - Up to two cores per Virtex-4 FX device
 - 702 DMIPS per core
 - Integrated 16Kbyte Instruction Cache
 - Integrated 16Kbyte Data Cache
- **Acceleration through Auxiliary Processor Unit (APU) Interface**
 - Provides direct access from FPGA fabric to PowerPC core
 - High-performance coprocessor support

More than 3 times faster than any soft μP

Fabric Resources

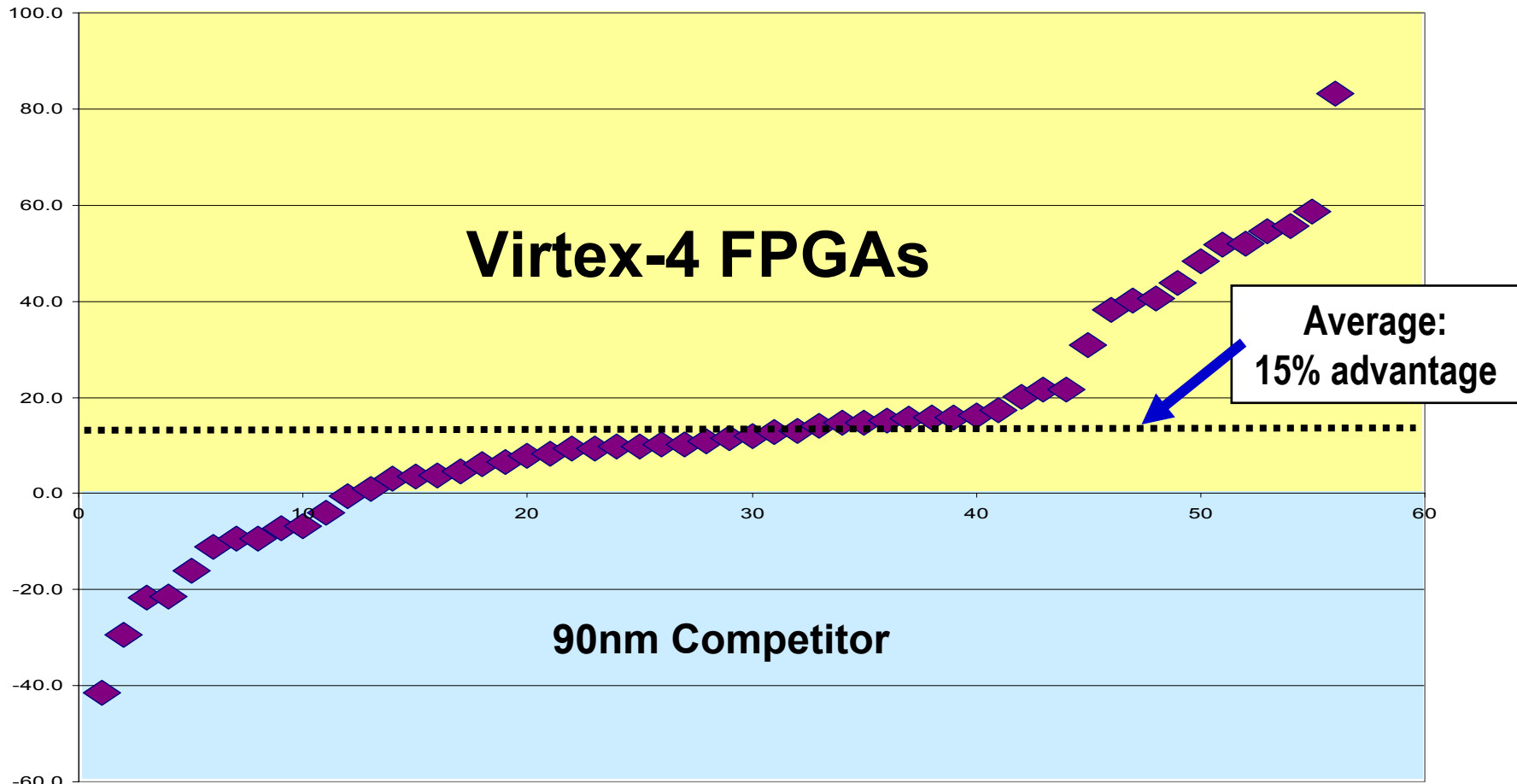


1 CLB = 4 Slices = 8 VLUTs

- Variable Look-Up-Table for:
 - Logic of 4, 5, 6 or 7 inputs
 - Distributed memory
 - 16-bit shift register, SRL16
- No shared inputs
 - Can pack unrelated functions
- Eight Flip-flops per CLB
- Fast carry

Logic and routing support 500 MHz operation

Benchmarks to Measure Fabric Performance



*Logic performance testing of fastest speed grades
using real customer designs and the best available tools*



Summary

- Xilinx is **First in 90nm FPGAs**
 - 100x more devices shipped than by all other PLD vendors combined
- Virtex-4 is the **world's fastest FPGA**
 - Traditional benchmarks show performance advantage in fabric
 - New functions enable breakthrough performance + reduced power + lower cost