



**TABLE 1—EDN PLD DIRECTORY: REPRESENTATIVE FPGAs**

Product line and configuration technology (antifuse, EPROM, flash, PROM, ROM, SRAM, or other)	Core operating voltages (V)	Packaging and pin-count options	Logic-cell count	Contents of each logic cell	LUT-derived memory density (bits)
<b>Actel</b>					
eX (antifuse)	2.5	CSP 49/128/180, TQFP 64/100	64 to 256 (register cell), 128 to 512 (combinatorial cell)	One register and one four-input multiplexer (register cell) or one three-input multiplexer, one OR gate, one AND gate, and one inverter (combinatorial cell)	NA
MX (antifuse)	3.3, 5	CQFP 208/256, PBGA 272, PLCC 44/68/84, PQFP 100/160/208/240, TQFP 176, VQFP 80/100/176	295 to 2438	One four-input multiplexer, one two-input AND gate, one two-input OR gate (C-module), one C-module plus one register (S-module), one seven-input AND gate, and one two-input XOR gate (D-module)	NA
ProASIC (flash)	2.5 to 3.3	BG 272/454, FG 144/676, PQ 208	5376 to 26,880	One three-input combinatorial- or sequential-logic cluster	NA
SX (antifuse)	3.3	FBGA 144, PBGA 313/329, PLCC 84, PQFP 208, TQFP 144/176, VQFP 100	256 to 1080 (register cell), 512 to 1800	One register and one four-input multiplexer (register cell) or one three-input multiplexer, one OR gate, one (combinatorial cell) AND gate, and one inverter (combinatorial cell)	NA
SX-A (antifuse)	2.5	CQFP 208/256, FBGA 144/256/484, PBGA 329, PQFP 208, TQFP 100/144/176	56 to 2012 (register cell), 512 to 4024 (combinatorial cell)	One register and one four-input multiplexer (register cell) or one three-input multiplexer, one OR gate, one AND gate, and one inverter (combinatorial cell)	NA
<b>Agere Systems</b>					
ORCA Series 2 (SRAM)	3.3, 5	EBGA 432, PBGA 256/352, PLCC 84, QFP 160, SQFP2 208/240/304, TQFP 100/144	499 to 3600	Four four-input LUTs, four registers, eight tristate buffers	6400 to 57,600
ORCA Series 3 (SRAM)	2.5, 3.3, 5	EBGA 432/600, PBGA 256/352, PBGAM 680, SQFP 208/240, TQFP 144	1152 to 11,552	Eight four-input LUTs, nine registers, 10 tristate bidirectional buffers, PAL-like logic for as-much-as-10-bit decoding, and AND-OR-INVERT logic	18,432 to 184,832
ORCA Series 4 (SRAM)	1.5	EBGA 432, FCBGA 1521, PBGA 352, PBGAM 680	624 to 4260	Eight four-input LUTs, nine registers, 10 tristate bidirectional buffers, PAL-like logic for as-much-as-10-bit decoding, and AND-OR-INVERT logic	79,872 to 591,360
ORLI10G (SRAM)	1.5	PBGAM 416/680	1296	Eight four-input LUTs, nine registers, 10 tristate bidirectional buffers, PAL-like logic for as-much-as-10-bit decoding, and AND-OR-INVERT logic	165,888
OR3LP26B (SRAM)	2.5	EBGA 432/680, PBGA 352, SQFP2 240	4032	Eight four-input LUTs, nine registers, 10 tristate bidirectional buffers, PAL-like logic for as-much-as-10-bit decoding, and AND-OR-INVERT logic	64,512
ORT4622 (SRAM)	2.5	EBGA 432, PBGAM 680	4032	Eight four-input LUTs, nine registers, 10 tristate bidirectional buffers, PAL-like logic for as much as 10-bit decoding, and AND-OR-INVERT logic	64,512
ORT82G5 (SRAM)	1.5	PBGAM 680	1296	Eight four-input LUTs, nine registers, 10 tristate bidirectional buffers, PAL-like logic for as-much-as-10-bit decoding, and AND-OR-INVERT logic	165,888
ORT8850 (SRAM)	1.5	EBGA 432, PBGA 256, PBGAM 680	624 to 2024	Eight four-input LUTs, nine registers, 10 tristate bidirectional buffers, PAL-like logic for as-much-as-10-bit decoding, and AND-OR-INVERT logic	259,072
<b>Altera</b>					
ACEX 1K (SRAM)	2.5	1-mm BGA, PQFP, TQFP (100 to 672 pins)	576 to 4992	One four-input LUT, one register, programmable carry chain, programmable cascade chain	NA
APEX 20K (SRAM)	2.5	1.27-mm BGA, PQFP, RQFP, TQFP (144 to 672 pins)	4160 to 16,640	One four-input LUT, one register, programmable carry chain, programmable cascade chain	NA
APEX 20KC (SRAM)	1.8	1-mm BGA, 1.27-mm BGA, PQFP, RQFP (208 to 1020 pins)	8320 to 51,840	One four-input LUT, one register, programmable carry chain, programmable cascade chain	NA
APEX 20KE (SRAM)	1.8	1-mm BGA, 1.27-mm BGA, PQFP, TQFP (144 to 1020 pins)	1200 to 51,840	One four-input LUT, one register, programmable carry chain, programmable cascade chain	NA
APEX II (SRAM)	1.5	1-mm BGA, 1.27-mm BGA (672 to 1508 pins)	16,640 to 89,280	One four-input LUT, one register, programmable carry chain, programmable cascade chain	NA

Dedicated-memory density (bits)	Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price range (end of 2001; 10,00 units; cheapest package; lowest speed; commercial temperature)
NA	NA			\$2.30 to \$6.30
2560 (MX 36 only)	256			\$2.90 to \$23
13, 824 to 64,512	2304	Dedicated FIFO control logic	Single-chip, live at power-up, in-system reprogrammable, design security, ASIC design flow	\$15 to \$100
NA	NA			\$7.50 to \$21.80
NA	NA			\$4.40 to \$23.10
NA	NA	NA	Full PCI compliance, 40-MHz configuration	\$4.90 to \$43
NA	NA	Microprocessor interface, programmable clock manager	Memory performance reaching 160 MHz	\$9.60 to \$206
73,728 to 221,184	9216	Microprocessor interface, programmable clock manager		\$41 to \$697
110,592	9216		Based on ORCA Series 4 architecture; 16-bit serial interface supports 622 Mbps for OC-192/STM-64 SONET, 645 Mbps for 10-Gigabit Ethernet, 667 Mbps for Strong FEC at OC-192; 781 Mbps for Super FEC (12.5 Gbps) at OC-192	\$177.90
NA	NA	Full-featured, 33/50/66-MHz, 32/64-bit PCI interface; four internal FIFOs (two 64×32 bits, two 16×64 bits); microprocessor interface; programmable clock manager	Based on ORCA Series 3 architecture	\$77.60
NA	NA	Full-duplex, four-channel, 622-Mbps backplane transceiver with CDR (as much as 2.5 Gbps when combined); pseudo-SONET plus FIFOs; microprocessor interface; framer programmable clock manager	Based on ORCA Series 3 architecture, power-down option for CDR receiver on per-channel basis, variety of backplane IP cores available	\$83.20
110,592	9216		Based on ORCA Series 4 architecture; variety of backplane IP cores available including POS-PHY, 10-Gigabit Ethernet, Fibre Channel, Infiniband interfaces	\$191.90
73,728 to 147,456	9216	Full-duplex, eight-channel, 850-Mbps backplane transceiver with CDR (as much as 6.2 Gbps when combined); pseudo-SONET framer plus FIFOs; microprocessor interface; programmable clock manager	Based on ORCA Series 4 architecture, power-down option for CDR receiver on per-channel basis, variety of backplane IP cores available	\$76.80 to \$369
12,288 to 49,152	2048		In-circuit reconfiguration, MultiVolt I/O support, JTAG support	\$3 to \$13
53,248 to 212,992	2048	One PLL	LVTTTL, LVCMOS, and PCI support; in-circuit reconfiguration; MultiVolt I/O support; JTAG support	\$44 to \$440
106,496 to 442,368	2048	Copper interconnects, two to four PLLs, 840-Mbps LVDS I/O buffers, embedded logic analyzer (SignalTap)	I/O standards support for SSTL, PCI, GTL+, AGP, CTT, LVPECL, LVCMOS, and LVTTTL; in-circuit reconfiguration; MultiVolt I/O support; JTAG support	\$45 to \$820
24,576 to 442,368	2048	Two to four PLLs, 840-Mbps LVDS I/O buffers, embedded logic analyzer (SignalTap)	I/O standards support for SSTL, PCI, GTL+, AGP, CTT, LVPECL, LVCMOS, and LVTTTL; in-circuit reconfiguration; MultiVolt I/O support; JTAG support	\$8 to \$550
425,984 to 1,523,712	4096	Four PLLs, eight global clocks, 1-Gbps LVDS I/O buffers, embedded logic analyzer (SignalTap)	Copper interconnects; I/O standards support for HyperTransport; SSTL, PCI, GTL+, AGP, CTT, LVPECL, LVCMOS, and LVTTTL; MultiVolt I/O support; JTAG support	\$290 to \$1450

**TABLE 1—EDN PLD DIRECTORY: FPGAs (CON'T)**

Product line and configuration technology (antifuse, EPROM, flash, PROM, ROM, SRAM, or other)	Core operating voltages (V)	Packaging and pin-count options	Logic-cell count	Contents of each logic cell	LUT-derived memory density (bits)
Excalibur (SRAM)	1.8		4160 to 38,400 327,680	One four-input LUT, one register, programmable carry chain, programmable cascade chain	NA
Mercury (SRAM)	1.8	1-mm BGA (484 to 780 pins)	4800 to 14,400	One four-input LUT, one register, programmable carry chain, programmable cascade chain	NA
<b>Atmel</b>					
AT6000 (SRAM)	3.3, 5	BQFP 132, PLCC 84, PQFP 208/240, TQFP 144, VQFP 100	1024 to 6400	Most functions of two and three inputs with or without D-type register, and tristate driver	NA
AT40Kxx (SRAM)	3.3, 5	Bare die, BGA 352, PLCC 84, PQFP 208/240/304, RQFP 100, TQFP 144, VQFP 100	256 to 2304	Two three-input LUTs or one four-input LUT with or without D-type register, plus multiplier AND gate, internal feedback, and tristate driver	NA
AT40KxxAL (SRAM)	3.3	Bare die, BGA 352, PLCC 84, PQFP 208/240/304, RQFP 100, TQFP 144, VQFP 100	256 to 2304	Two three-input LUTs or one four-input LUT with or without D-type register, plus multiplier AND gate, internal feedback, and tristate driver	NA
AT40KxxAX (SRAM)	1.8	Bare die, BGA 352, PLCC 84, PQFP 208/240/304, RQFP 100, TQFP 144, VQFP 100	512 to 6400	Two three-input LUTs or one four-input LUT with or without D-type register, plus multiplier AND gate, internal feedback, and tristate driver	NA
AT94KxxAL FPSLIC (SRAM)	3.3	Bare die, BGA 256, PLCC 84, PQFP 208, TQFP 144, VQFP 100	256 to 2304	Two three-input LUTs or one four-input LUT with or without D-type register, plus multiplier AND gate, internal feedback, and tristate driver	NA
AT94KxxAX FPSLIC (SRAM)	1.8	Bare die, BGA 256, PLCC 84, PQFP 208, TQFP 144, VQFP 100	512 to 6400	Two three-input LUTs or one four-input LUT with or without D-type register, plus multiplier AND gate, internal feedback, and tristate driver	NA
AT94SxxAL Secure FPSLIC (SRAM)	3.3	BGA 256	256 to 2304	Two three-input LUTs or one four-input LUT with or without D-type register, plus multiplier AND gate, internal feedback, and tristate driver	NA
AT94SxxAX Secure FPSLIC (SRAM)	1.8	BGA 256	512 to 6400	Two three-input LUTs or one four-input LUT with or without D-type register, plus multiplier AND gate, internal feedback, and tristate driver	NA
<b>QuickLogic</b>					
Eclipse (antifuse)	2.5	BGA 484/516/672, FPBGA 280, PQFP 208	960 to 4032	Two six-input AND gates, four two-input AND gates, seven two-input multiplexer, two registers, as many as six independent outputs	NA
pASIC 1 (antifuse)	5	CPGA 68/84/144, CQFP 160/208, PLCC 44/68/84, PQFP 208, TQFP 100/144	96 to 768	Two six-input AND gates, four two-input AND gates, three two-input multiplexer, one register, as many as five independent outputs	NA
pASIC 2 (antifuse)	5 or 3.3	PBGA 256, PLCC 84, PQFP 208, TQFP 100/144	192 to 672	Two six-input AND gates, four two-input AND gates, six two-input multiplexers, one register, as many as five independent outputs	NA
pASIC 3 (antifuse)	3.3	PBGA 256/456, PLCC 68/84, PQFP 208, TQFP 100/144	96 to 1584	Two six-input AND gates, four two-input AND gates, six two-input multiplexers, one register, as many as five independent outputs	NA
QuickDSP (antifuse)	2.5	BGA 484/516/672, FPBGA 280, PQFP 208	960 to 4032	Two six-input AND gates, four two-input AND gates, seven two-input multiplexers, two registers, as many as six independent outputs	NA
QuickFC (antifuse)	3.3	PBGA 456, PQFP 208	560	Two six-input AND gates, four two-input AND gates, six two-input multiplexers, one register, as many as five independent outputs	NA

Dedicated-memory density (bits)	Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price range (end of 2001; 10,00 units; cheapest package; lowest speed; commercial temperature)
53,248 to	2048	Embedded ARM and MIPS microprocessors, four PLLs, four global clocks, 840-Mbps LVDS I/O buffers, embedded logic analyzer (SignalTap)	Microprocessor peripherals; I/O standards support for SSTL, PCI, GTL+, AGP, CTT, LVPECL, LVCMOS, and LVTTTL; in-circuit reconfiguration; MultiVolt I/O support, JTAG support	\$265 to \$925
49,152 to 114,688	4096	Two to four PLLs, four global clocks, 1.25-Gbps CDR and LVDS I/O buffers, embedded logic analyzer (SignalTap), quad-port RAM	Carry-select look-ahead mode, multiplier mode, MultiVolt I/O operation, in-circuit reconfiguration, JTAG support, I/O row bands, array-driver technology	\$120 to \$350
NA	NA		Dynamically reconfigurable to individual-core-cell level	\$6 to \$40
2048 to 18,432	128		Dynamically reconfigurable to core-cell level, very low power consumption	\$5 to \$50
2048 to 18,432	128		Dynamically reconfigurable to core-cell level, very low power consumption	\$4 to \$50
4608 to 51,200	128		Dynamically reconfigurable to core-cell level, very low power consumption	\$4 to \$50
2048 to 18,432	128	25-MHz AVR RISC microcontroller with dual UARTs, three timers, two-wire serial bus, 8×8 two-cycle multiplier, two I/O ports, two oscillator circuits, four external interrupts, a watchdog timer, as much as 36 kbytes of program and data SRAM	Dynamically reconfigurable to core-cell level from AVR; very low power consumption; simple built-in interfaces between AVR, FPGA, and memory	\$10 to \$50
4608 to 32,768	128	25-MHz AVR RISC microcontroller with dual UARTs, three timers, two-wire serial bus, 8×8 two-cycle multiplier, two I/O ports, two oscillator circuits, four external interrupts, a watchdog timer, as much as 36 kbytes of program and data SRAM	Dynamically reconfigurable to core-cell level from AVR; very low power consumption; simple built-in interfaces between AVR, FPGA, and memory	\$7 to \$50
2048 to 18,432	128	25-MHz AVR RISC microcontroller with dual UARTs, three timers, two-wire serial bus, 8×8 two-cycle multiplier, two I/O ports, two oscillator circuits, four external interrupts, a watchdog timer, as much as 36 kbytes of program and data SRAM	Includes serial EEPROM for holding secure program and data code as a multichip module; dynamically reconfigurable to core-cell level from AVR; very low power consumption; simple built-in interfaces between AVR, FPGA, and memory	\$13 to \$58
4608 to 32,768	128	25 MHz AVR RISC microcontroller with dual UARTs, three timers, two-wire serial bus, 8×8 two-cycle multiplier, two I/O ports, two oscillator circuits, four external interrupts, a watch dog timer, as much as 36 kBytes of program and data SRAM	Includes serial EEPROM for holding secure program and data code as a multichip module; dynamically reconfigurable to core-cell level from AVR; very low power consumption; simple built-in interfaces between AVR, FPGA, and memory	\$9 to \$58
46,080 to 82,944	2304	Four PLLs	Support for multiple single and differential I/O standards, maximum 600-MHz register-to-register performance	\$15.95 to \$79.09
NA	NA	Also available in military-plastic-packaged, military-ceramic-packaged, and MIL-STD-883 versions		\$8.95 to \$69.35
NA	NA		Instant-on capability, high security and reliability, low power, supports 5V, 3.3V, and mixed-voltage systems	\$14.85 to \$59.82
NA	NA		High performance (400 MHz), instant-on capability, high security and reliability, low power, supports 5V, 3.3V, and mixed-voltage systems, also available in a military-plastic-packaged version	\$4.50 to \$36.90
46,080 to 82,944	2304	Four PLLs, 10 to 18 hardware ECUs providing extremely fast multiplication and addition for DSP applications	Support for multiple single and differential I/O standards, maximum 600-MHz register-to-register performance	\$19.95 to \$98.87
25,344	1152	Fibre Channel encoder/decoder supports high-speed serial applications at 2.5 Gbps maximum	High performance (400 MHz), instant-on capability, high security and reliability, low power	\$29.50 to \$45

**TABLE 1—EDN PLD DIRECTORY: FPGAs (CON'T)**

Product line and configuration technology (antifuse, EPROM, flash, PROM, ROM, SRAM, or other)	Core operating voltages (V)	Packaging and pin-count options	Logic-cell count	Contents of each logic cell	LUT-derived memory density (bits)
QuickPCI (antifuse)	3.3	CQFP 208, PBGA 256/456/484, PQFP 208, TQFP 144	266 to 1302	Two six-input AND gates, four two-input AND gates, six two-input multiplexers, one register, as many as five independent outputs	NA
QuickRAM (antifuse)	3.3	CPGA 84/144/256, CQFP 100/208, PBGA 256/456, PLCC 68/84, PQFP 208/240, TQFP 100/144	160 to 1584	Two six-input AND gates, four two-input AND gates, six two-input multiplexers, one register, as many as five independent outputs	NA
QuickSD (antifuse)	2.5	FPBGA 280, PBGA 484/516/672, PQFP 208	960 to 4032	Two six-input AND gates, four two-input AND gates, seven two-input multiplexers, two registers, as many as six independent outputs	NA
<b>Triscend</b>					
A7 CSoC (SRAM)	2.5	BGA 324/484, PQFP 208	512 to 3200	Four-input LUT, D-type flip-flop with clock enable and asynchronous set or reset, carry/cascade logic, connections to internal address/data bus, debugging logic, optional LUT configuration as 8-bit serial-in/serial-out shift register	8192 to 51,200
E5 CSOC (SRAM)	3.3	BGA 484, LQFP 128, PQFP 208	256 to 3200	Four-input LUT, D-type flip-flop with clock enable and asynchronous set or reset, carry/cascade logic, connections to internal address/data bus, debugging logic, optional LUT configuration as 8-bit serial-in/serial-out shift register	4096 to 51,200
<b>Xilinx</b>					
Spartan (SRAM)	5	BGA 256, PLCC 84, PQFP 208, PQFP 240, TQFP 144, VQFP 100	238 to 1862	Four-input LUT, carry logic, storage element (either edge-triggered D-type flip-flop or level-sensitive latch)	3200 to 25,088
Spartan-XL (SRAM)	3.3	BGA 256, CSP 144/280, PLCC 84, PQFP 208/240, TQFP 144, VQFP 100	238 to 1862	Four-input LUT, carry logic, storage element (either edge-triggered D-type flip-flop or level-sensitive latch)	3200 to 25,088
Spartan-II (SRAM)	2.5	CSP 144, FBGA 256/456, PQFP 208, TQFP 144, VQFP 100	432 to 5292	Four-input LUT, carry logic, storage element either edge-triggered D-type flip-flop (or level-sensitive latch)	3072 to 37,632
Virtex-II (SRAM)	1.5	BF 957, BG 575/728, CS 144, FF 896/1152/1517, FG 256/456/676	576 to 138,240	Four-input LUT, one register, one carry-chain multiplexer, other logic	8192 to 1,966,080

Note: Information in this table, including pricing, comes directly from the vendors. Please confirm information before finalizing your design.

Dedicated-memory density (bits)	Size of each dedicated memory block (bits)	Other embedded functions	Other notable features	Price range (end of 2001; 10,00 units; cheapest package; lowest speed; commercial temperature)
9216 to 25,344	1152	32- and 64-bit PCI target and master/target controllers	Seven devices span a range of PCI functions at speeds reaching 75 MHz; also available in military-plastic-packaged, military-ceramic-packaged, and MIL-STD-883 versions	\$9.95 to \$65
9216 to 25,344	1152		High performance (400 MHz), instant-on capability, high security and reliability, low power	\$5.95 to \$49.50
55,296 to 82,944	2304	As many as eight Bus LVDS SERDES blocks supporting 1-to-1, 4-to-1, 7-to-1, 8-to-1, and 10-to-1 serial/parallel and parallel/serial conversion	Support for multiple single and differential I/O standards, maximum 600 MHz register-to-register performance	\$24.75 to \$64.90
131,072	131,072		Supported by most ARM-based development tools and RTOS environments, pin-compatible package footprint between family members, 2.5 or 3.3V I/O buffers, ASIC-based cost-reduction path available	\$19.95 (A7S20)
65,536 to 524,288	65,536 to 524,288		Supported by most 8051/8052 compilers and debuggers, pin-compatible package footprint between family members, 5V-tolerant I/O buffers, ASIC-based cost-reduction path available	\$4.80 to \$18.75
NA	NA	CLBs include two four-input LUTs, one three-input LUT, and two registers; broad set of AllianceCORE and LogiCore IP available	System performance beyond 80 MHz, fully PCI compliant, internal tristate-bus capability	\$4.95 to \$20.25
NA	NA	CLBs include two four-input LUTs, one three-input LUT, and two registers; broad set of AllianceCORE and LogiCore IP available	Includes Spartan features plus 3.3V supply for low power with 5V-tolerant I/Os, power-down input, faster carry logic, 5 and 3.3V PCI-compatible	\$3.75 to \$14.25
16,384 to 57,344	4096	Four DLLs, four primary-global-clock nets plus 24 secondary-clock nets, true dual-port block RAM, 16 I/O standards	System performance to 200 MHz, fully PCI-compliant, partial reconfiguration, power-down mode	\$5.25 to \$19.45
73,728 to 3,538,944	18,432	Four to 12 digital clock managers, 16 global-clock multiplexer buffers, two separate carry chains, sum-of-product support, 18×18-bit multipliers	IP-Immersion architecture, Xcite digitally controlled impedance, Select I/O-Ultra to 1108 user I/Os, active interconnect	\$13.25 to \$1834 (not including 8 million- and 10 million-gate devices)