

Super PLL Application Guide

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Introduction

Fujitsu's Super PLLs are designed to be used in frequency synthesizers for programmable and fixed local oscillator generation in modern radio systems. Applications range from 1V, 100 MHz pagers to 3V operation for Global System for Mobile Communications (GSM), and other cellular and cordless standards. These standards include applications in the second ISM band between 2.4 GHz and 2.483 GHz. Figure 1 shows a simplified representation of a PLL frequency synthesizer. The shaded blocks represent those integrated in a Super PLL Integrated Circuit (IC).

To complete the subsystem, the PLL IC requires the addition of an external loop filter, Voltage Controlled Oscillator (VCO) and reference source. The reference source can be an external Temperature Compensated Crystal Oscillator (TCXO) or, if the accuracy of the generated carrier is not critical, a simple external

crystal. The E, C, and MB15U10 series have the built-in oscillator circuitry. The VCOs in most modern radio systems require very high performance. These modular devices usually come in a sealed can and are obtainable from several manufacturers.

The loop filter can be either passive or active. In most cases, a simple, passive, low-pass filter constructed from a few resistors and capacitors can be used.

All new Fujitsu PLLs operate from a single 3V power supply (or less). They are available in 8-, 16-, or 20-pin Shrink Small Outline Package (SSOP) packages. The E and F series are available in the proprietary Bump Chip Carrier (BCC) package. The BCC package provides enhanced RF performance, coupled with up to 50% savings in the Printed Circuit Board (PCB) area.

In the case of programmable devices (all except the S series), the exact frequency is selected by setting bits in internal registers via a 3-wire serial bus.

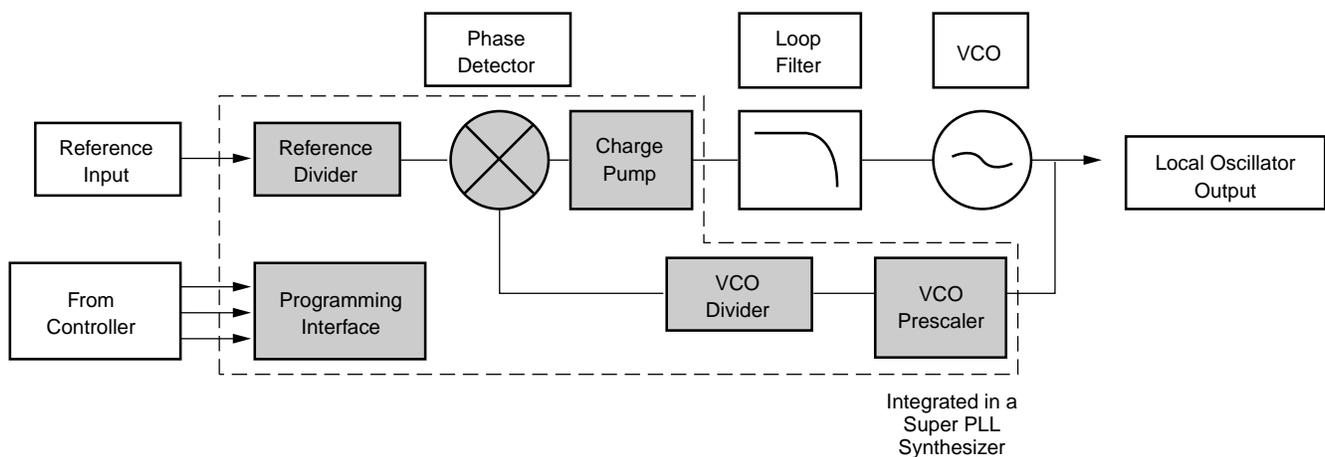


Figure 1. Simplified PLL Synthesizer

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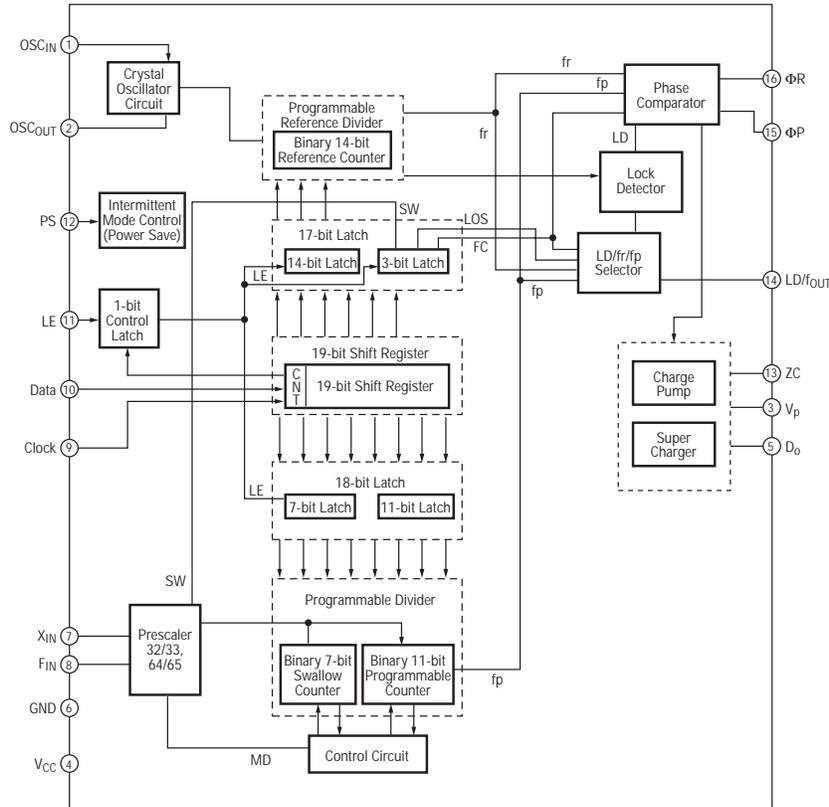


Figure 2. MB15E07L Architecture

Fujitsu PLL Architecture

Figure 2 illustrates the architecture of the MB15E07L, a typical Fujitsu Super PLL.

With minor differences, all the Super PLLs in the current Fujitsu product offering have similar architectures.

Reference Oscillator

All Super PLL devices have an input port to provide the PLL with a reference signal. Some have a built-in oscillator circuit. The internal oscillator circuit, shown in Figure 2, can be configured as an input buffer amplifier (Figure 3), or as a crystal oscillator (Figure 4).

Figure 3 shows the reference source AC coupled to the input pin (OSC_{IN}), while the output pin (OSC_{OUT}) is left open. 1000pF is the maximum value that should be used.

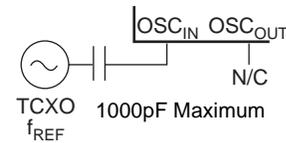


Figure 3. Reference Source

In Figure 4, the internal oscillator generates the reference signal for the PLL with the external capacitors and crystal defining the frequency of operation. Be sure to minimize the size of the capacitors to ground, including the strays caused by the PCB. Verify that the total load on each pin does not exceed 30pF. The values of C1 and C2 set the load on the crystal.

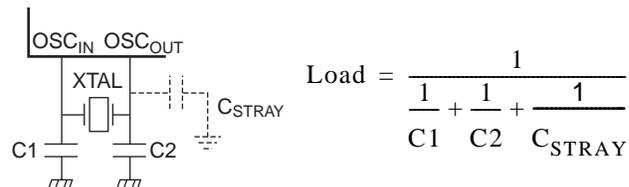


Figure 4. The Internal Oscillator Generating the Reference Signal

C1 or C2 can be trimmed to make small adjustments to the frequency.

Due to package size limits, the F and S series have only a reference oscillator input pin. Therefore, only the configuration shown in Figure 3 is possible. Figure 5 illustrates a typical representation of the reference input frequency range versus sensitivity.

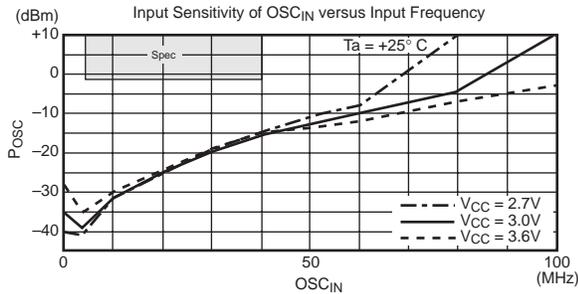


Figure 5. OSC_{IN} Input Sensitivity

Figure 6 shows an example of the input impedance of the input buffer.

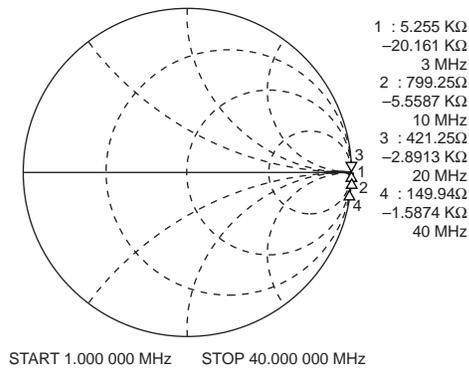


Figure 6. OSC_{IN} Input Impedance

Reference Divider

The reference input is divided by the programmable reference divider/counter, hereafter referred to as the *R-counter*. This signal is applied to the phase detector for comparison with the divided VCO signal. All Super PLLs divide the VCO signal using a prescaler, described on the next page.

VCO Input Buffer

The VCO input is applied to the IC through a high-frequency differential buffer, as shown in Figure 7. The output level of the VCO should be adjusted to be near the minimum level required for the input buffer. Always operate close to the minimum level, because this helps minimize crosstalk. Crosstalk could cause unnecessary spurious signals on the output signal.

AC coupling is required, because the input buffer generates its own input bias point. Figure 8 shows an example of the input sensitivity of the input buffer.

Figure 9 shows an example of the input buffer's input impedance.

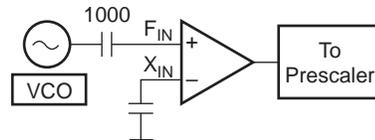


Figure 7. Prescaler Input Buffer

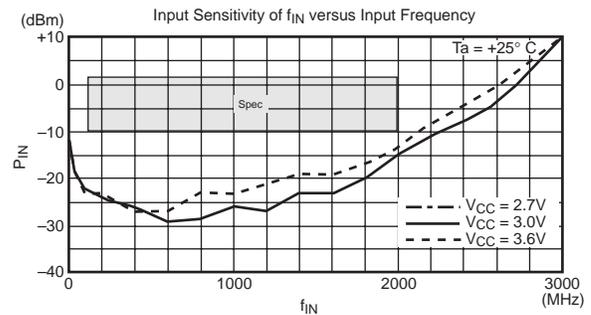


Figure 8. Prescaler Input Sensitivity

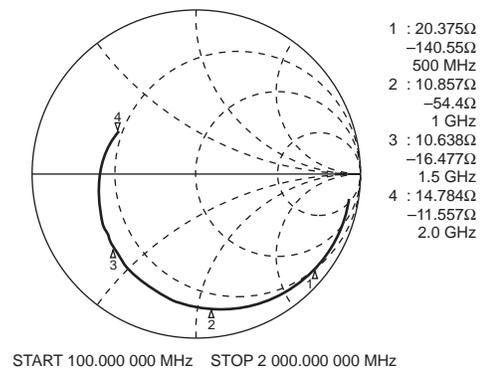


Figure 9. Prescaler Input Impedance

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Prescaler/VCO Divider

All Super PLLs divide the VCO signal using a prescaler. The prescaler is a bipolar circuit in all devices, except the C series. In all devices, except the MB15U10, the prescaler has at least two dividing ratios (hereafter known as M and $M+1$). This type of prescaler is known as *dual modulus*.

Following the prescaler is a CMOS counter (hereafter referred to as the N -counter), which divides the signal down to the comparison frequency of the reference signal. When in lock mode, the frequencies at the phase detector are equal.

In a single modulus system, the frequency generated is provided by:

$$f_{VCO} = f_{REF} \left(\frac{N \cdot M}{R} \right)$$

In a dual modulus system, the prescaler divider ratio is dynamically altered during the course of an (R/f_{REF}) period by the use of a controlling swallow counter (hereafter known as the A -counter). The value of the A -counter is programmed via the serial interface to a value less than that of the N -counter. At the start of an (R/f_{REF}) or (N/f_{VCO}) period, the prescaler is divided by the dividing ratio $(M+1)$ until the A -counter reaches its programmed value. Thereafter, the prescaler divides by M . This leads to the following formula, which defines the frequency generated:

$$f_{VCO} = f_{REF} \frac{(NM + A)}{R}$$

To use a dual modulus system as a single modulus, the A -counter value is set to 0. Most Super PLLs have two dual modulus prescalers, which can be statically selected via the programming interface. In the example of MB15E07L (Figure 2), the prescaler can be configured as either 32/33 or 64/65. The N -, A -, and R -counters have wide programming ranges to permit use in a wide variety of applications.

Charge Pump/Phase Detector

In order to produce an error signal, the divided VCO frequency and the reference signal are applied to the phase detector. The error signal is then used to control the charge pump operation.

The phase detector is a Type 4 phase/frequency detector.

This means that when the loop is very far from lock mode, the frequencies are compared until both frequencies are equal. The phase can then be compared. The Fujitsu Super PLL series features a proprietary charge pump architecture, the Supercharger. The Supercharger provides excellent phase noise performance, low spurious output, and fast channel-hop lock-in times. The Supercharger charge pump is a balanced-current source type. Figure 10 shows the typical circuit topology. Figure 11 illustrates an example of the output currents, varying with applied voltage on the output.

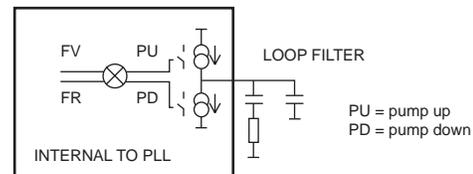


Figure 10. Charge Pump Topology

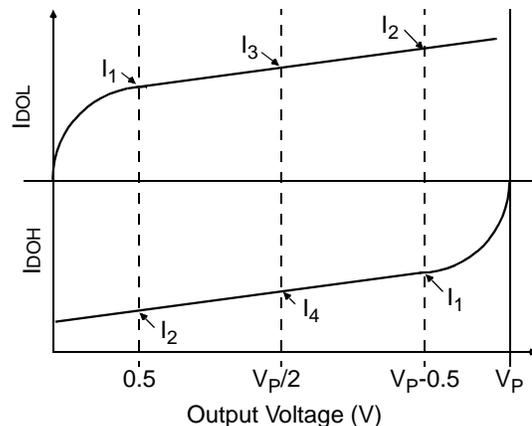


Figure 11. Charge Pump Output Currents

Features of Selected PLL Series

Table 1. The MB15E Series

Part Number	Max. Input Frequency (MHz)	Features	I _{CC} (mA)	V _{CC} (V)	Package	Application	Prescaler		Program Counter	Swallow Counter	Ref. Counter Type	Ref. Counter Range
							Div. Ratio 1	Div. Ratio 2				
MB15E03	1200	PS/ZC	3.5	3	16-pin SSOP, BCC	PDC, GSM, ADC	64/65	128/129	5-2047	0-127	Programmable	5-16383
MB15E03L	1200	PS/ZC	2.5	3	16-pin SSOP, BCC	PDC, GSM, IS-54, IS-95	64/65	128/129	5-2047	0-127	Programmable	5-16383
MB15E03SL	1200	PS/ZC	2.0/2.5	2.7/3	16-pin SSOP, BCC	PDC, GSM, IS-54, IS-95	64/65	128/129	3-2047	0-127	Programmable	3-16383
MB15E05	2000	PS/ZC	6	3	16-pin SSOP, BCC	DCS, PCS, DECT	64/65	128/129	5-2047	0-127	Programmable	5-16383
MB15E05L	2000	PS/ZC	4	3	16-pin SSOP, BCC	DCS, PCS, DECT	64/65	128/129	5-2047	0-127	Programmable	5-16383
MB15E05SL	2000	PS/ZC	3/3.5	2.7/3	16-pin SSOP, BCC	DCS, PCS, DECT	64/65	128/129	3-2047	0-127	Programmable	3-16383
MB15E07	1800	PS/ZC	8	3	16-pin SSOP, BCC	DCS, PCS	32/33	64/65	5-2047	0-127	Programmable	5-16383
	2500	PS/ZC	8	3	16-pin SSOP, BCC	DCS, PCS, WLAN	—	64/65	5-2047	0-127	Programmable	5-16383
MB15E07L	2000	PS/ZC	4.5	3	16-pin SSOP, BCC	DCS, PCS, WLAN	32/33	64/65	5-2047	0-127	Programmable	5-16383
	2500	PS/ZC	4.5	2.3/3	16-pin SSOP, BCC	DCS, PCS, WLAN	—	64/65	5-2047	0-127	Programmable	5-16383
MB15E07SL	2000	PS/ZC	3.5/4	2.7/3	16-pin SSOP, BCC	DCS, PCS, WLAN	32/33	64/65	3-2047	0-127	Programmable	3-16383
	2500	PS/ZC	3.5/4	2.7/3	16-pin SSOP, BCC	DCS, PCS, WLAN	—	64/65	3-2047	0-127	Programmable	3-16383

The E series of PLLs features a hardware Power Save (PS) mode controlled from a single pin and a hardware charge pump output selection controlled from a single pin (ZC).

The PS mode enables the switching of the PLL in and out of its standby status without using the 3-wire bus, thus saving time (and therefore power) when switching.

Using the ZC pin permits the user to switch the charge pump into a high-impedance mode. This switching is useful for open-loop modulation schemes in which the VCO is set to a particular frequency and the loop is opened to allow the VCO to run free. Stringent requirements are thus placed on the leakage current of the components connected to the tuning pin on the VCO. The loop filter capacitors must exhibit low leakage characteristics. The ZC pin enables this high-impedance mode without the requirement to access the 3-wire bus.

The E series also features a separate charge pump power supply pin (Vp). This allows the user to operate the digital part of the PLL device at 3V, thus saving power while operating the analog part at a higher voltage. This permits a greater VCO tuning range. The Vp pin must be operated at a voltage greater than or equal to V_{CC} and less than 6V.

Of particular interest is the MB15ExxSL series of devices. These single PLLs feature very low operating current specifications and use a highly balanced charge pump with a selectable 6 mA or 1.5 mA output. The user can select the charge pump current via the 3-wire programming interface. This increased design flexibility helps to optimize PLL performance.

The E series is available in 16-pin SSOP and 16-pin BCC-S packages.

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Table 2. The MB15F Series

Part Number	Max. Input Frequency (MHz)	Features	I _{CC} (mA)	V _{CC} (V)	Package	Application	Prescaler		Program Counter	Swallow Counter	Ref. Counter Type	Ref. Counter Range
							Div. Ratio 1	Div. Ratio 2				
MB15F02	1200	PS	3.5	3.5	16-pin SSOP, BCC	GSM, 800PDC, IS-54, IS-95	64/65	128/129	5-2047	0-127	Programmable	5-16383
	500	PS	2.5	3			16/17	32/33				
MB15F02L	1200	PS	2.5	3	16-pin SSOP, BCC	GSM, 800PDC, IS-54, IS-95	64/65	128/129	5-2047	0-127	Programmable	5-16383
	250	PS	1.5	3			16/17	32/33				
MB15F02SL	1200	PS Prog. CP	3.0	3	16-pin SSOP, BCC	GSM, 800PDC, IS-54, IS-95	64/65	128/129	3-2047	0-127	Programmable	3-16383
	500	PS Prog. CP					8/9	16/17				
MB15F03	2000	PS	6	3	16-pin SSOP, BCC	DCS, PCS, DECT, PHS, IS-54, IS-95	64/65	128/129	5-2047	0-127	Programmable	5-16383
	500	PS	3	3			16/17	32/33				
MB15F03L	1800	PS	3.5	3	16-pin SSOP, BCC	DCS, DECT, PHS, IS-54, IS-95	64/65	128/129	5-2047	0-127	Programmable	5-16383
	250	PS	1.5	3			16/17	32/33				
MB15F03SL	1750	PS Prog. CP	3.5/4.0	2.7/3	16-pin SSOP, BCC	DCS, DECT, PHS, IS-54, IS-95	64/65	128/129	3-2047	0-127	Programmable	3-16383
	600	PS Prog. CP					8/9	16/17				
MB15F04	2000	PS	5	3	20-pin SSOP	DCS, DECT, PHS, PCS, IS-54, IS-95	64/65	128/129	5-2047	0-127	Programmable	5-16383
	2000	PS	6	3			64/65	128/129				
MB15F05L	1800	PS	3.4	3	16-pin SSOP, BCC	PHS	64/65	128/129	5-2047	0-127	Programmable	5-16383
	233.15	PS	1.6	3			16/17					
MB15F07SL	1100	PS Prog. CP	4.0	3	16-pin SSOP, BCC	GSM, 800ODC, IS-54, IS-95	64/65	128/129	3-2047	0-127	Programmable	3-16383
	1100	PS Prog. CP					64/65	128/129				
MB15F08SL	2500	PS Prog. CP	5.5	3	16-pin SSOP, BCC	DCS, PCS, WLAN	32/33	64/65	3-2047	0-127	Programmable	3-16383
	1200	PS Prog. CP					16/17	32/33				

The F series of PLLs are high-performance dual-channel PLLs. They feature a hardware Power Save (PS) mode. In some cases, such as the MB15F02, the channels support two separate frequencies:

- A Radio Frequency (RF) to generate a first Local Oscillator (LO)
- An Intermediate Frequency (IF) channel to generate a second LO

In other dual PLLs, such as the MB15F07SL, the channels support two RF frequencies generating the LOs for both the transmit and receive chains. The F series is thus ideal for double-superhet radio systems.

Of particular interest is the MB15FxxSL series of dual PLLs. These feature very low-operating current specifications and use a highly balanced charge pump with a selectable 6mA or 1.5mA output. User can select the charge pump current via the 3-wire programming interface. This increased design flexibility helps to optimize PLL performance.

The F series is available in 16-pin SSOP and 16-pin BCC-D packages. The pin count is limited in a dual PLL. Therefore, the reference input, PS and power supply each use a single pin.

Table 3. The MB15C Series

Part Number	Max. Input Frequency (MHz)	Features	I _{CC} (mA)	V _{CC} (V)	Package	Application	Prescaler		Program Counter	Swallow Counter	Ref. Counter Type	Ref. Counter Range
							Div. Ratio 1	Div. Ratio 2				
MB15C02	220	PS	1.5-2.0	0.6-1.2	16/20-pin SSOP	Pagers	64/65	—	5-4095	0-63	Programmable	16-16383
	330	PS	2.0-2.7	1.0-1.8	16/20-pin SSOP	Pagers	64/65	—	5-4095	0-63	Programmable	16-16383
MB15C03	90	PS	1.0-1.5	0.5-1.0	16-pin SSOP	Pagers	64/65	—	5-4095	0-63	Programmable	5-16383
	120	PS	1.2-1.2	0.7-1.4	16-pin SSOP	Pagers	64/65	—	5-4095	0-63	Programmable	5-16383

The C series PLLs, comprising MB15C02 and MB15C03, represent Fujitsu's PLL offering for low-voltage applications. They are constructed in a CMOS process that has a low-threshold voltage. The CMOS process enables operation down to a power supply voltage of 1V. The prescaler is also constructed in CMOS. These parts are suited to Pager applications using POCSAG, FLEX, or the European ERMES standard.

The MB15C02 features a PS mode controlled by a PS pin. The MB15C02 operates from a single 1V supply, permitting operation using a single battery cell without the use of a DC/DC converter. The MB15C02 is available in 16- or 20-pin SSOP packages.

The MB15C03 also has both a PS mode controlled by a single pin and a separate charge pump power supply pin. This permits a larger tuning range VCO to be used while still maintaining low-power consumption. The MB15C03 is available in a 16-pin SSOP package.

Table 4. The MB15S Series

Part Number	Max. Input Frequency (MHz)	Features	I _{CC} (mA)	V _{CC} (V)	Package	Application	Prescaler		Program Counter	Swallow Counter	Ref. Counter Type	Ref. Counter Range
							Div. Ratio 1	Div. Ratio 2				
MB15Sxx	300	MASK	3.5	3	8-pin SOP/SSOP	IF LO	16/17	32/33	5-4095	0-31	Mask	0-4095
MB15S01	233.15	FIXED	3.5	3	8-pin SSOP	PHS	16/17	—	291	7	Fixed	384
	259.2	FIXED	3.5	3	8-pin SSOP	PHS	16/17	—	33	12	Fixed	40
MB15S02	284	FIXED	3.5	3	8-pin SSOP	GSM	16/17	—	17	12	Fixed	13
	116	FIXED	3.5	3	8-pin SSOP	GSM	16/17	—	7	4	Fixed	13
MB15S03	178	FIXED	3.5	3	8-pin SSOP	PDC	16/17	—	27	13	Fixed	32
	129.55	FIXED	3.5	3	8-pin SSOP	PDC	16/17	—	161	15	Fixed	256

The MB15Sxx series is a fixed-frequency synthesizer. This single-frequency PLL has an integrated prescaler that can operate at frequencies up to 300 MHz. The reference, the VCO and the pulse swallow counters, have fixed ratios that the user can select via a metal mask option at production time. One or two fixed frequencies can be programmed and switched via a single control pin. To choose a single frequency, the user can select the hardware PS option. The part is therefore customized for each application and eliminates the need for a programming controller.

For compactness, the devices are packaged in a choice of either 8-pin Small Outline Package (SOP) or 8-pin SSOP.

A typical application for an MB15Sxx series PLL would be one in which high levels of isolation are required between RF and IF PLLs. A dual PLL would not be used. When a Fujitsu MB15E07L is used for an application in the 2.0 GHz band, using an MB15Sxx series PLL is a good low cost way to generate the IF frequency (see Figure 12).

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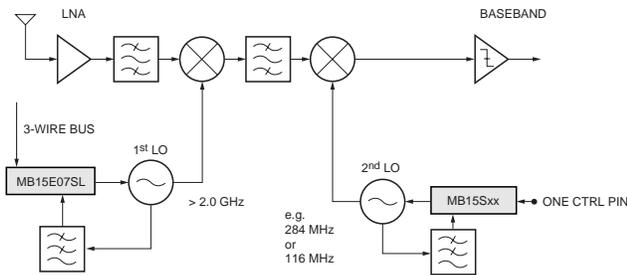


Figure 12. Simplified 2.4 GHz Dual Superhet Receiver

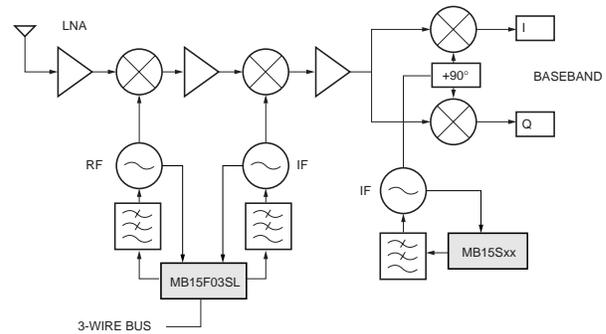


Figure 13. Simplified 3-LO System

Figure 13 shows an example of a more complicated application for the S series. Some systems are designed with multiple IFs, indicating that multiple local oscillators are required. Using a dual PLL is the most cost-effective way to produce the first two LOs,

but a third one must be generated. A standard fully programmable, single PLL is not required for the third LO, because it is fixed in frequency and does not require programmability.

Table 5. The MB15U Series

Part Number	Max. Input Frequency (MHz)	Features	I _{CC} (mA)	V _{CC} (V)	Package	Application	Prescaler		Program Counter	Swallow Counter	Ref. Counter Type	Ref. Counter Range
							Div. Ratio 1	Div. Ratio 2				
MB15U10	1100	PS Prog. CP	3.5/5.5	3/5	20-pin SSOP	GSM, 800PDC, IS-54, IS-95	—	—	1024-131071	—	Programmable	6-4095
	1100	PS Prog. CP	3.5/5.5	3/5			—	—	1024-131071	—	Programmable	6-4095
MB15U36	2000	PS Prog. CP	3.5/6	3/5	16-pin SSOP	CATV/STB, DECT, DCS, PCS, GSM, IS-54, IS-95	64/65	128/129	3-2047	0-127	Programmable	3-32767
	1200	PS Prog. CP	2.5/3	3/5			64/65	128/129	3-2047	0-127	Programmable	3-32767

The MB15U10 is a dual-frequency synthesizer with both channels operating at up to 1.1 GHz. This makes the MB15U10 suitable for a radio system that requires separate LOs for the first receive (RX) and transmit (TX) down conversions. The MB15U10 device is pin-compatible to the UMA1015MA. The part features:

- Separate V_p and V_{CC} inputs
- A PS function actuated either by a pin (PS) or by software control
- A charge pump that allows the conversion gain to be set via an external resistor

Power supply can be between 2.6 and 5.5V. The MB15U10 is available in a 20-pin SSOP package.

The MB15U36 is a dual RF frequency synthesizer with the RF1 PLL operating at 2.0 GHz and the RF2 PLL at 1.2 GHz. It operates over a wide supply voltage range of 3.0 to 5.0 V. It features low operating current and utilizes a highly balanced Charge Pump with a selectable 1.0 mA or 4.0 mA output when using a 3V supply. A programmable Power Save feature allows independent shut-down control of either PLL to minimize power drain in portable applications.

The MB15U36 is pin and function compatible with the LMX2336 dual PLL. It is available in a 20-pin SSOP package.

RF Layout for Good Results

In order to obtain a reliable and high-performance RF design, several PCB layout guidelines must be followed. RF signal traces should be kept short and, where possible, terminated with 50 Ω . This is relatively easy to do when using a multilayer board. Careful decoupling of the power supplies is also important. Both large-value and small-value decoupling capacitors should be placed as close as possible to the IC power-supply pins. These devices act as a low-impedance path to ground for any stray high-frequency transients. Normally, a value of around 100 pF is used for this purpose. The ground connection should be laid out as a “ground plane” to avoid generating stray inductance that can negate the effect of the capacitors, or worse, generate a resonant circuit that can lead to parasitic oscillations. Connecting to the ground plane from the bond pin can have an inductance of 1 nH.

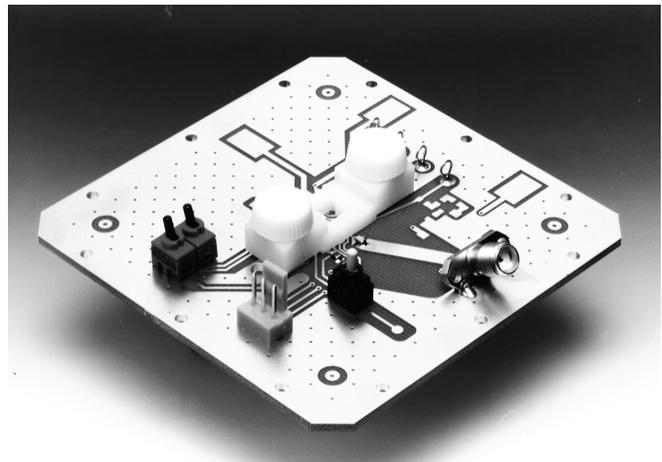
As a rule, the synthesizer supply should be separated from any digital circuitry present in the design. Particularly sensitive is the ground connection to the loop filter. To achieve the best performance, the loop filter should be constructed from film capacitors, which exhibit a high Q factor, and low leakage.

Measurement Hints

When making measurements, using a shielded chamber is best. A low-noise signal generator, or the actual TCXO from the system to be designed, must be used for the OSC_{IN} signal. Ground loops can create 60 Hz spurs and harmonics around the carrier signal. Some measurement instruments, especially those equipped with a cathode ray display, can generate higher frequency spurs. For a test setup, additional inductors in the power rails can improve the noise performance. For phase noise measurements, all generators should be connected to the same reference timebase.

Evaluation Systems

Designing a complex subsystem, such as a PLL, is no easy task. Therefore, Fujitsu has made available an evaluation system to aid in the development of reliable frequency synthesizers. Each evaluation system consists of two PCBs, controlling software, and instructions. The first PCB, common to all PLLs, is used as a programming interface between the PC and the second RF PCB. This second RF PCB is laid out to allow the target MB15xxxx part to be optimized as a frequency synthesizer for the chosen application. The RF board is only semi-populated, which allows the user to configure it to fit the application.



Support is provided through RF evaluation boards.

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Fujitsu Super PLL Evaluation Board Lineup

Table 6 lists the Fujitsu Super PLLs currently supported by evaluation systems. All of them, as well as their RF boards, are used in conjunction with the MB1500EB00 programming board.

Table 6. Evaluation Boards

Singles	f_{IN} (max, MHz)	I_{CC} (mA)	Package	Evaluation Board
MB15E03 (L, SL)	1200	3.5 (2.5, 2.5)	16SSOP 16BCC-S	MB1500EB01 MB1500EB01B
MB15E05 (L, SL)	2000	6.0 (4.0, 3.0)	16SSOP 16BCC-S	MB1500EB01 MB1500EB01B
MB15E07 (L, SL)	2500	8.0 (4.5, 4.0)	16SSOP 16BCC-S	MB1500EB01 MB1500EB01B
MB15S01	270	3.5	8SSOP	MB1500EB02
MB15S02	300	3.5	8SSOP	MB1500EB02
MB15S03	200	3.5	8SSOP	MB1500EB02
Duals	f_{IN} (max, MHz)	I_{CC} (mA)	Package	Evaluation Board
MB15F02 (L, SL)	1200 500	5.5 (4.0, 3.0)	16SSOP 16BCC-D	MB1500EB13 MB1500EB013B
MB15F03 (L, SL)	2000 500	9.0 (5.0, 4.0)	16SSOP 16BCC-D	MB1500EB13 MB1500EB013B
MB15F05L	1800 233.15	5.0	16SSOP 16BCC-D	MB1500EB13 MB1500EB013B
MB15F07SL	600 1100	4.0	16SSOP 16BCC-D	MB1500EB13 MB1500EB013B
MB15F08SL	1200 2500	5.5	16SSOP 16BCC-D	MB1500EB13 MB1500EB013B
MB15U10	1100 1100	7.0	20SSOP	MB1500EB12
MB15U36	2000 1200	6	20SSOP	MB1500EB36

PLL Programming

Swallow Counter Calculations

PLLs with swallow counters have the following frequency counters/dividers on the chip:

- Input counter/prescaler (R) (also called the *reference counter*)
- Dual modulus counter/prescaler (M) and (M+1)
- Program counter (N)
- Swallow counter (A)

The reference frequency, divided by the reference counter (R), sets channel spacing.

$$f_{\text{channel spacing}} = f_{\text{REF}} / R$$

The RF input prescaler is configured as a dual modulus prescaler; that is, it can be set to divide by (M) or (M+1) by setting a control bit. The swallow counter controls the modulus (M+1) or (M) of the prescaler. Both the swallow counter and the program counter are both driven at the same time from the output of the dual modulus prescaler. The swallow counter counts for only a portion of the program counter's interval. For example, the swallow counter initially sets the dual modulus prescaler to divide by (M+1). When the swallow counter reaches its programmed value (A), it switches the dual modulus prescaler to divide by (M). For this reason, the swallow counter is always programmed to a lower number (A < N) than the program counter.

The swallow counter permits the program counter to count two different frequencies during the interval (N). The proportion of (M+1) and (M) counts during the program counter cycle permits the synthesis of many different families of frequencies.

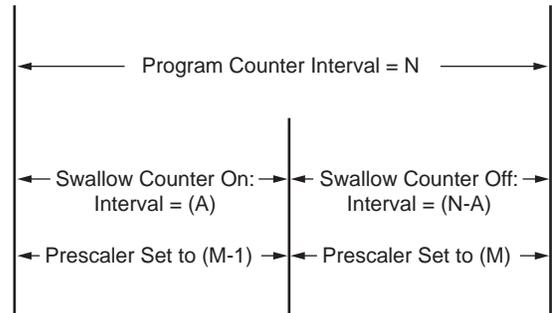


Figure 14. Prescaler M Under the Control of Swallow Counter A

Figure 14 shows the relationship among the (M+1), (M), (N), and (A) counters:

- While the swallow counter is on, the division ratio = (M+1) * (A)
- While the swallow counter is off, the division ratio = (M) * (N-A)
- The total number of pulses counted during the interval N is the sum: (M+1) * (A) + (M) * (N-A) = (N * M) + A

The output frequency of a swallow counter PLL is therefore:

$$f_{\text{VCO}} = ((N * M) + A) * (f_{\text{REF}} / R)$$

Note: A must be less than N.

Figure 15 shows the BiCMOS PLL.

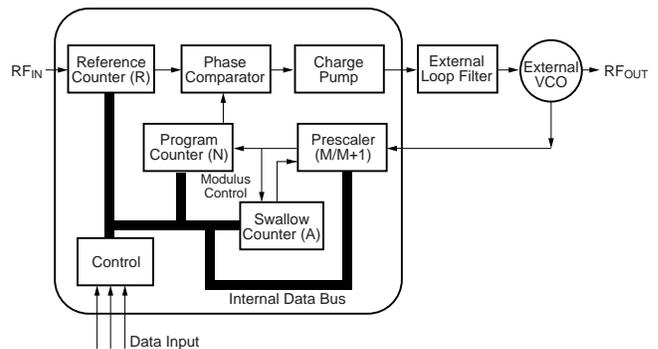


Figure 15. Swallow Counter BiCMOS PLL

Super PLL Application Guide

Programming Example: FM Broadcast Receiver Local Oscillator

Design Criteria

- Frequency Range: 87.9 MHz to 107.9 MHz
- Channel Spacing: 200 kHz
- IF: 10.7 MHz
- Reference Oscillator: 40 MHz
- High Side Injection

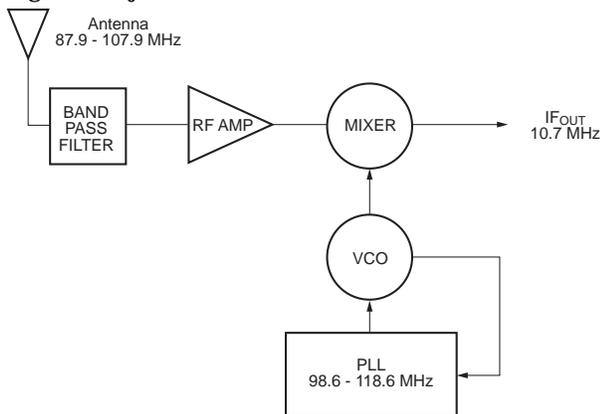


Figure 16. FM Broadcast LO Generation

Follow these steps:

1. Perform the preliminary calculations:
 - a. PLL lowest output frequency = $(87.9 + 10.7) = 98.6$ MHz
 - b. PLL highest output frequency = $(107.9 + 10.7) = 118.6$ MHz
 - c. Number of channels = $((107.9 - 87.9) / 0.2) + 1 = 101$
 - d. R counter = $40 \text{ MHz} / 0.2 \text{ MHz} = 200$
2. Select the dual modulus prescaler:

$M = 15/16$
3. Program the counter interval.
 - a. Lowest count = $(98.6 / 0.2) = 493$
 - b. Highest count = $(118.6 / 0.2) = 593$
4. Find the starting value of the swallow counter.
 - a. Lowest count = 493
 - b. $M = 15$
 - c. Total interval count = $(N * M) + A = 493$
 - d. Let $A = 0$
 - e. Then $493 = (15 * N)$
 - f. $N = 493/15 = 32.867$

- g. Set $N = \text{INT}(N) = 32$ (see Note)
- h. Find $A = 493 - (32 * 15) = 493 - 480 = 13$

Note: The INT function returns the integer value of a decimal number.

5. Test the starting values (channel 1).
 - a. $M = 15$
 - b. $N = 32$
 - c. $A = 13$
 - d. Condition $(A < N)$ is met
 - e. Total interval count = $(15 * 32) + 13 = 493$
 - f. Reference frequency = 0.2 MHz
 - g. Lowest frequency = $(493 * 200,000) = 98.6$ MHz
6. To increment the channels, increment Swallow Counter A by 1. For example, calculate channel 2 as follows:
 - a. $M = 15$
 - b. $N = 32$
 - c. $A = 14$
 - d. Condition $(A < N)$ is met
 - e. Total interval count = $(15 * 32) + 14 = 494$
 - f. Reference frequency = 0.2 MHz
 - g. Next frequency = $(494 * 200,000) = 98.8$ MHz
7. By incrementing (A), the channels from 1 to 19 are synthesized. When $A = 32$, the condition $(A < N)$ fails and the PLL can no longer generate the desired frequencies. At this point, the N counter must be changed to another value as follows:
 - a. Channel 20 count = $512 = (N * M) + A$
 - b. Let $A = 0$
 - c. Then $N = 512 / 15 = 34.13333$
 - d. Set $N = \text{INT}(34.13333) = 34$
 - e. Find $A = 512 - (15 * 34) = 2$
8. Test the values for channel 20.
 - a. $M = 15$
 - b. $N = 34$
 - c. $A = 2$
 - d. Total interval count = $(N * M) + A = (15 * 34) + 2 = 512$
 - e. Channel 20 frequency = $(512 * 200,000) = 102.4$ MHz
9. To synthesize channels 20 to 49, increment A by 1 for each successive channel. When channel 50 is reached, the condition $(A < N)$ again fails and a new number for N is calculated. This process continues until all 101 channels are synthesized. Repeating the calculation can lead to a simple program to find all the values of N and A for a given M.

Programming Example: High-Frequency Hopping Receiver

Design Criteria

- Frequency Range: 2399 MHz to 2501 MHz
- Channel Spacing: 1000 kHz
- IF: 480 MHz
- Reference Oscillator: 12 MHz
- Low Side Injection

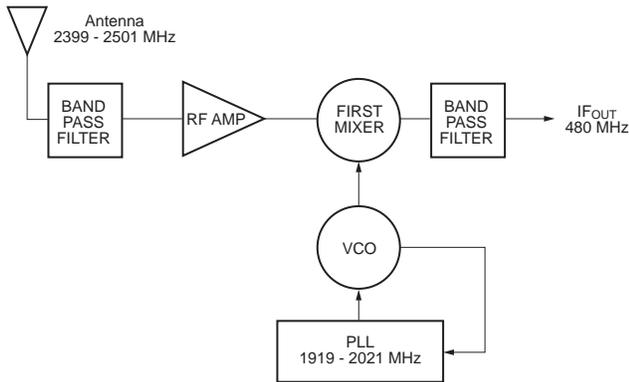


Figure 17. High Frequency LO Generation

Follow these steps:

1. Perform the preliminary calculation.
 - a. PLL lowest output frequency = $(2399 - 480) = 1919$ MHz
 - b. PLL highest output frequency = $(2501 - 480) = 2021$ MHz
 - c. Number of channels = $((2500 - 2400) / 1.0) + 1 = 103$
 - d. R counter = $12 / 1 = 12$
2. Select the dual modulus prescaler.

$M = 15/16$
3. Program the counter interval.
 - a. Lowest count = $(1919 / 1.0) = 1919$
 - b. Highest count = $(2021 / 1.0) = 2021$

4. Find the starting value of the swallow counter.
 - a. Lowest count = 1919
 - b. $M = 15$
 - c. Total interval count = $(N * M) + A = 1919$
 - d. Let $A = 0$
 - e. Then $1919 = (15 * N)$
 - f. $N = 1919 / 15 = 127.933$
 - g. Set $N = \text{INT}(127.9333) = 127$ (see Note)
 - h. Find $A = 1919 - (127 * 15) = 1919 - 1905 = 14$
 - i. $A = 14$

Note: The INT function returns the integer value of a decimal number.

5. Test the starting values (channel 1).
 - a. $M = 15$
 - b. $N = 127$
 - c. $A = 14$
 - d. Condition $(A < N)$ is met
 - e. Total interval count = $(15 * 127) + 14 = 1919$
 - f. Reference frequency = 1.0 MHz
 - g. Lowest frequency = $(1920 * 1,000) = 1,919,000$ kHz = 1919 MHz
6. To increment the channels, increment A by 1. For example, calculate channel 2 as follows:
 - a. $M = 15$
 - b. $N = 127$
 - c. $A = 15$
 - d. Condition $(A < N)$ is met
 - e. Total interval count = $(15 * 127) + 15 = 1920$
 - f. Reference frequency = 1.0 MHz
 - g. Channel 2 frequency = $(1920 * 1,000) = 1,920,000$ kHz = 1920 MHz

The swallow counter (A) needs to run between 14 and 116 to synthesize all 101 channels. A is always more than N; therefore, changing the value of M or N is not necessary.

Super PLL Application Guide

Loop Filter Design

Because of its low cost and low noise, it is desirable to use a simple passive loop filter. Figure 18, shows the configuration of a typical loop filter.

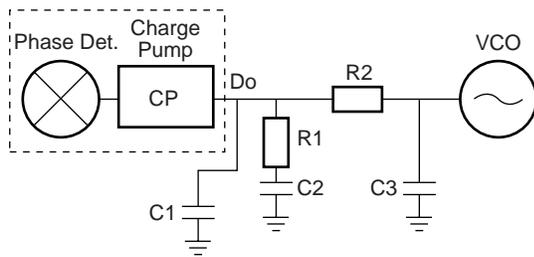


Figure 18. Loop Filter

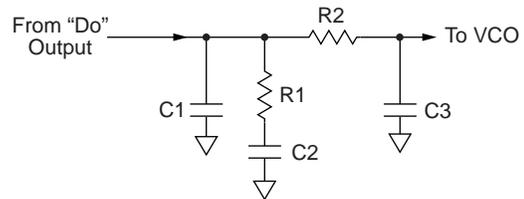
C1, C2, C3, R1, and R2 form a third order filter. The VCO creates an extra pole. Therefore, the complete structure of the loop filter creates a fourth order loop. The components R1 and C2 represent the core of the loop filter, whereby the other components—C1 and the cascaded low-pass R2 and C3—are used to further enhance the system performance by adding higher order attenuation. The user can omit low-pass filter, R2-C3, in many applications. Consider the following when optimizing any PLL frequency synthesizer:

- The time it takes to step from one frequency to another
- The suppression of reference side bands
- The minimum in-band phase noise to obtain

As the order of the loop increases, the calculation of the loop filter components becomes unmanageable. In the following calculation, only the components R1 and C2 are generated from a theoretical approach. C1 is generated by a simple rule of thumb. The low-pass filter can be dimensioned to have a 3 dB cutoff, approximately a decade away from that of the loop bandwidth.

Fujitsu PLL Loop Filter Calculations

Typical Loop Filter



Follow these steps:

1. Determine the maximum dividing ratio, N.

$$N = \frac{\text{Maximum VCO Frequency}}{\text{Channel Spacing}}$$

2. Calculate f_n (natural frequency).

$$f_n = \frac{-1}{2\pi \cdot ts \cdot \xi} \cdot \ln\left(\frac{f_a}{f_{step}}\right)$$

Start with a damping factor (ξ) of 0.7 and “ts” less than .002 second.

3. Calculate capacitor C2.

$$C2 = \frac{I_{cp} \cdot K_{vco}}{N \cdot (2\pi \cdot f_n)^2}$$

4. Calculate resistor R1.

$$R1 = 2 \cdot \xi \cdot \sqrt{\frac{N}{I_{cp} \cdot K_{vco} \cdot C2}}$$

5. Calculate capacitor C1.

$$C1 = \frac{C2}{10}$$

Note: C1 can be adjusted to optimize the PLL performance.

6. Calculate R2 and C3 filters.

R2 and C3 are used to reduce any “spurs” caused by the reference frequency. Verify that the product of R2 and C3 is at least 1/10 the product of C2 and R1.

Terms

f_{step}	Maximum frequency step, or hop, to a new frequency – in Hz
t_s	Desired time for the carrier to step to a new frequency – in seconds
f_a	Frequency accuracy of the carrier within the desired time after a “step” or hop – in Hz
ξ	Damping factor
f_n	Natural frequency – in Hz
I_{cp}	Charge pump output current, in Amps
K_{VCO}	VCO sensitivity in Hz/V
N	Divide ratio-carrier frequency/reference frequency
\ln	Natural LOG

Loop Filter Design Example

The first step in designing a filter is to specify the system. This example assumes a channelized system of which locking time is the most critical. This is applicable to any radio standard based on Frequency Division Multiple Access/Time Division Multiple Access (FDMA/TDMA). Specification of hopping time requires the definition of three parameters:

f_{step} (Hz)	Frequency hopping step; taken from the lowest frequency required in the radio system to the highest required
T (s)	Hopping time; the maximum allowable time taken to switch between the channels farthest apart. As a rule of thumb, the highest lock speed achievable with conventional; for example, non-fractional-N dual modulus systems, is around 300 μ s.
f_a (Hz)	Frequency accuracy to desired frequency; for example, how close the carrier must be to the desired frequency when hopping time is measured.

Example:

$$\text{let } f_{\text{step}} = 1005-1031 = 26 \text{ MHz}$$

$$f_a = 1 \text{ kHz}, T = 450 \mu\text{s}$$

Extract two more parameters from the data supplied by the manufacturers of the components used:

K_v (Hz/V)	The conversion gain of the VCO employed.
I_{cp} (mA)	The DC charge pump current as measured at the PLL output. Measurement conditions are usually specified as being the current drawn to ground or V_{CC} when the voltage at the charge pump output is held at $1/2$ the V_{CC} .

If the charge pump currents are not equal, calculate the complete gain by adding the current of the positive source to that of the negative source, and dividing by two.

Select the channel spacing of the system. This sets the maximum frequency at which the phase detector can resolve phase differences between the two signals. It is desirable to make the phase detector operate at as high a frequency as possible:

The higher the reference frequency, the lower the output phase noise within the loop bandwidth.

After selecting the channel spacing, calculate the N divider ratio. Taking the frequency and dividing by the channel spacing results in the highest N -counter setting. For example:

$$\text{Highest Frequency} = 1031 \text{ MHz}$$

$$\text{Channel Spacing} = 200 \text{ kHz}$$

$$N = 1031 \times 10^6 \div 200 \times 10^3$$

$$N = 5155$$

In this case, N represents the combined N (programmable divider) and M (prescaler) divide ratios. It does not matter if the resulting number is not a factor of the smallest prescaler dividing ratio, because the dual-modulus control logic takes care of the exact division ratios.

Step-by-Step Procedure

The following is a step-by-step procedure in the design of a typical Loop Filter:

Parameters

- VCO Frequency Range: 1005 to 1031 MHz
- VCO Tuning Sensitivity (K_{VCO}): 35 MHz/V
- Channel Spacing: 200 kHz
- Damping Factor (ξ): 0.707
- Charge Pump Output Current (I_{cp}): 10 mA
- Maximum Step Frequency (f_{step}): 26 MHz
- Step Switching Time (t_s): 450 μ s
- Frequency Accuracy after Step (f_a): 1 kHz

Super PLL Application Guide

Follow these steps:

1. Determine the maximum dividing ratio, N.

$$N = \frac{\text{Maximum VCO Frequency}}{\text{Channel Spacing}}$$

$$N = \frac{1031}{200e^3} = 5155$$

2. Determine the “natural frequency”, f_n (Loop Frequency).

$$f_n = \frac{-1}{6.28 \times 450e^{-6} \times 0.707} \times \ln\left(\frac{1000}{26e^6}\right)$$

$$f_n = 5088 \text{ Hz}$$

3. Determine C2.

$$C2 = \frac{0.01 \times 35e^6}{5155 \times (6.28 \times 5088)^2}$$

$$C2 = 0.0665 \mu\text{F}$$

4. Determine R1.

$$R1 = 2 \times 0.707 \times \sqrt{\frac{5088}{0.01 \times 35e^6 \times 0.0665 \times 10^{-6}}}$$

$$R1 = 665$$

5. Determine C1.

$$C1 = \frac{C2}{10}$$

$$C1 = 0.0066 \mu\text{F}$$

6. Determine R2 + C3.

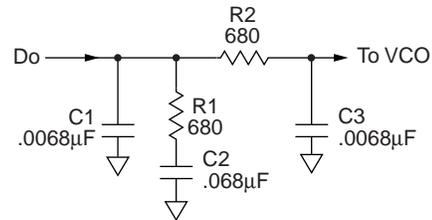
$$R2 = R1$$

$$R2 = 665$$

$$C3 = \frac{C2}{10}$$

$$C3 = 0.0066 \mu\text{F}$$

The final circuit using standard value components:



Loop Bandwidth

Calculate the approximate loop bandwidth as follows:

$$\begin{aligned} \text{Loop Bandwidth} &= \frac{(2\pi) \cdot f_n}{2} \left(\xi + \frac{1}{4\xi} \right) \text{Hz} \\ &= \frac{6.28 \times 5088}{2} \left(0.707 + \frac{1}{4 \times 0.707} \right) \\ &= 15976.32 \times (0.707 + 0.356) \\ &= 15976.32 \times 1.060 \\ &= 16944.5 \text{ Hz} \end{aligned}$$

Recommended Texts:

Frequency Synthesizer Design Handbook

James A. Crawford (Artech House)

Phaselock Techniques

FM. Gardner (John Wiley and Sons)

Digital PLL Frequency Synthesizers Theory and Design

U.L. Rhode (Englewood Cliffs)

Application Benchmarks

- This section details basic PLL performance results.
- All measurements were executed using an HP-4352B VCO-PLL signal analyzer.
- Each example can be further optimized in the user's exact system.
- The evaluation board used is an MB1500EB01.

Super PLL Application Guide

Design Example 1

V_{CC} :	3V
V_p, V_{VCO} :	5V
Comparator Frequency:	200 kHz
Reference Oscillator:	19.8 MHz
RF Out:	1018 MHz
Ambient Temperature:	25° C
VCO: Z-Comm V583ME04	$K_V = 35 \text{ MHz/V}$
f_a :	1000 Hz
T (Hopping Time):	450 μ s
Damping Factor:	.7

Parts List

C2	10 nF
C3	10 μ F
C4	100 pF
C5	33 pF
C6	33 pF
C10	100 pF
C11	10 μ F
C12, C13	30 pF
R3	0 Ω
R4	51 Ω
R5	47 k Ω
R6	47 k Ω
R7	47 k Ω
R8	18 Ω
R9	18 Ω
R10	18 Ω

Loop Filter

C7	.0068 μ F
C8	.068 μ F
C9	1000 pF
R1	3300 Ω
R2	680 Ω

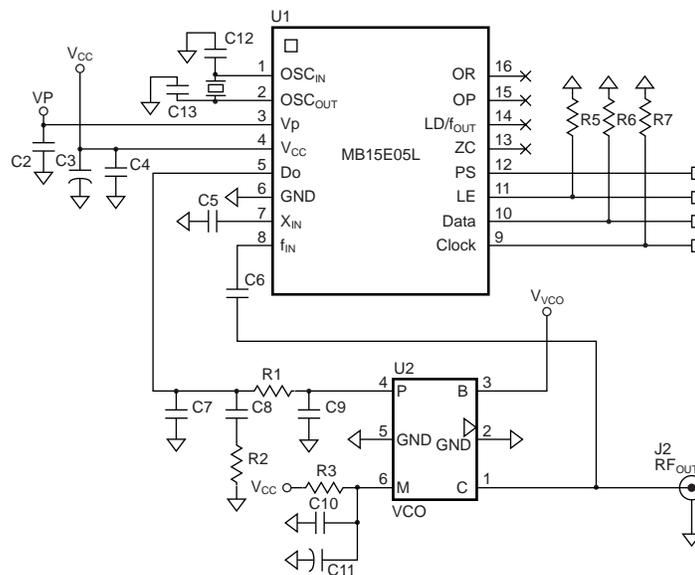


Figure 19. Application Circuit, GSM High Side Injection

Test Results at 1080 MHz

Phase Noise Performance within the Loop = -80.5 to -83.6 dBc/Hz

Spurious Performance at 200 kHz from the Carrier = -75.2 dBc

Hopping Time

1005.4 MHz to 1030.6 MHz = $368.5\mu\text{s}$

1030.6 MHz to 1005.4 MHz = $317.5\mu\text{s}$

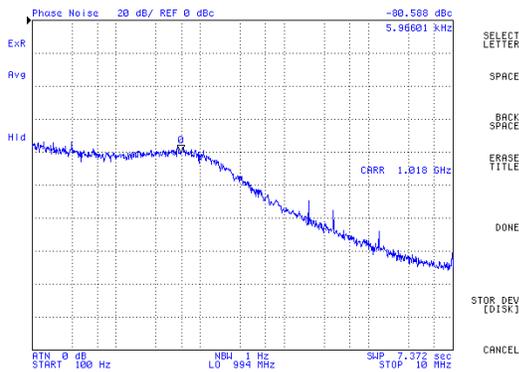


Figure 20. Phase Noise Performance C/N = -80.6 dBc/Hz
Maximum within the Loop Bandwidth

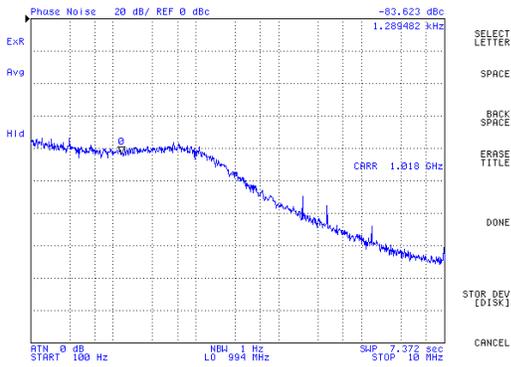


Figure 21. Phase Noise Performance C/N = -83.6 dBc/Hz
Minimum within the Loop Bandwidth

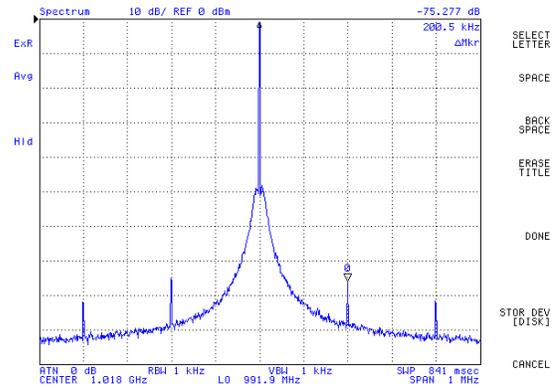


Figure 22. Spurious Performance at 1018 MHz = -75.2 dBc

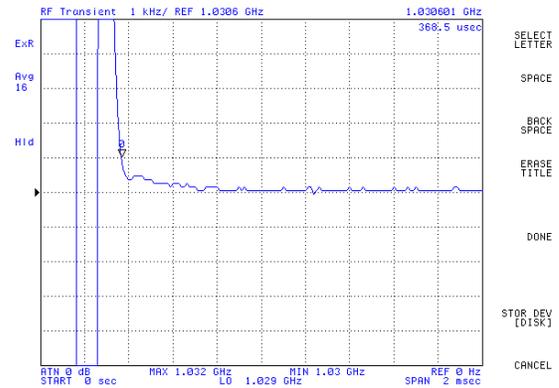


Figure 23. Hopping Time Step 1005.4 MHz
to 1030.6 MHz = $368.5\mu\text{s}$

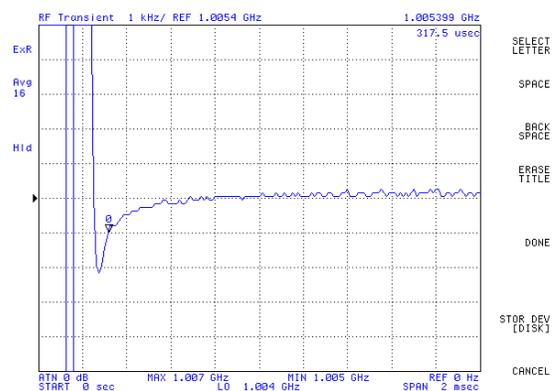


Figure 24. Hopping Time Step 1030.6 MHz
to 1005.4 MHz = $317.5\mu\text{s}$

Super PLL Application Guide

Design Example 2

V_{CC} :	3V
V_p, V_{VCO} :	4V
Comparator Frequency:	30 kHz
Reference Oscillator:	19.8 MHz
RF Out:	872.64 MHz
Ambient Temperature:	25° C
VCO: Z-Comm V582ME02	$K_V = 50 \text{ MHz/V}$
f_a :	1000 Hz
T (Hopping Time):	2ms
Damping Factor:	.85

Parts List

C2	10 nF
C3	10 μ F
C4	100 pF
C5	33 pF
C6	33 pF
C10	100 pF
C11	10 μ F
C12, C13	30 pF
R3	0 Ω
R4	51 Ω
R5	47 k Ω
R6	47 k Ω
R7	47 k Ω
R8	18 Ω
R9	18 Ω
R10	18 Ω

Loop Filter

C7	.015 μ F
C8	.47 μ F
C9	6800 pF
R1	3000 Ω
R2	600 Ω

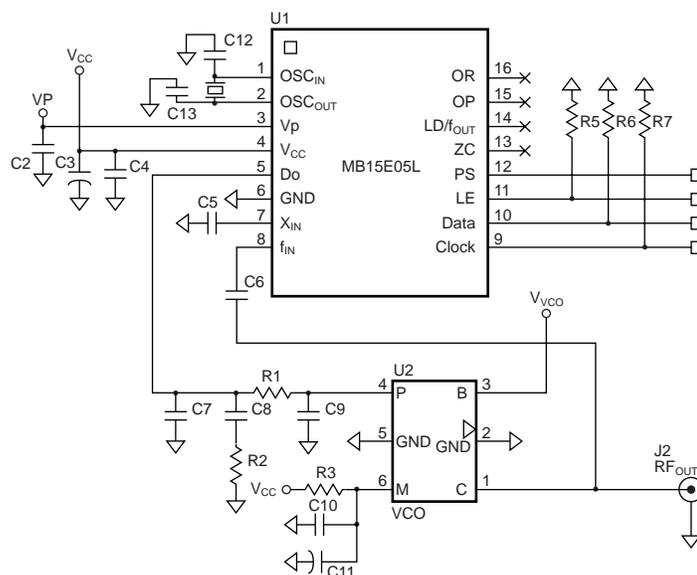


Figure 25. Application Circuit, Digital European Cordless Telephone (DECT) Low Side Injection

Test Results at 872.64 MHz

Phase Noise Performance within the Loop = -71.7 to -75.1 dBc/Hz

Spurious Performance at 30 kHz from the Carrier = -80.0 dBc

Hopping Time

860.07 MHz to 884.94 MHz = 1.43ms

884.94 MHz to 860.07 MHz = 1.84ms

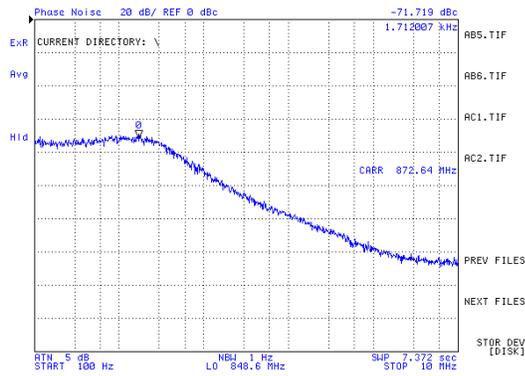


Figure 26. Phase Noise Performance C/N = -71.7 dBc/Hz
 Maximum within the Loop Bandwidth

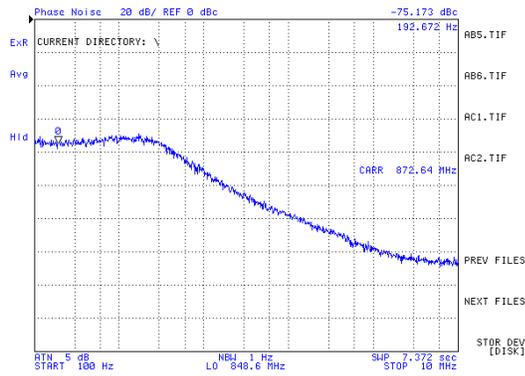


Figure 27. Phase Noise Performance C/N = -75.1 dBc/Hz
 Minimum within the Loop Bandwidth

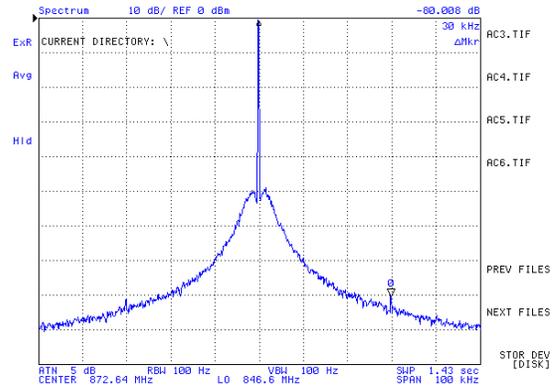


Figure 28. Spurious Performance at 872.64 MHz = -80.0 dBc

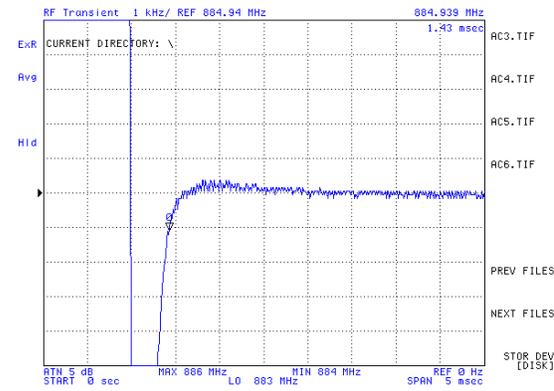


Figure 29. Hopping Time Step 860.06 MHz
 to 884.94 MHz = 1.43 ms

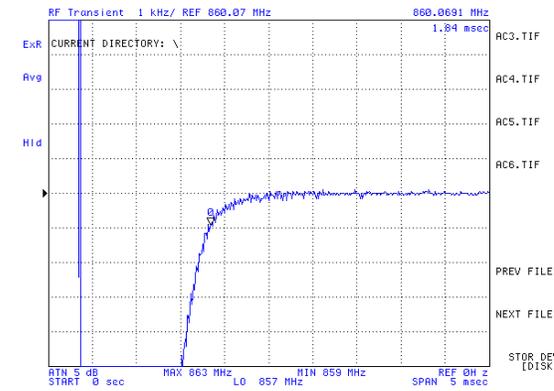


Figure 30. Hopping Time Step 884.94 MHz
 to 860.07 MHz = 1.84 ms

Super PLL Application Guide

Design Example 3

RF Section

V _{CC} :	3V
D _O :	6 mA
Comparator Frequency:	200 kHz
Reference Oscillator:	19.8 MHz, -3 dBm
RF Out:	1775 MHz
Ambient Temperature:	25° C
VCO: Z-Comm V613ME04:	K _V = 21 MHz/V
f _a :	1000 Hz
T _s (Hopping Time):	750 μs
Damping Factor:	.707

IF Section

D _O :	6 mA
Comparator Frequency:	50 kHz
IF _{OUT} :	232 MHz
VCO: Z-Comm V240ME01	25 MHz
Damping Factor:	.707

Parts List

C1	1000 pF
C2	100 pF
C3	22 mfd/6v
C4	.01μF
C5	1000 pF

Parts List (Continued)

C12	1000 pF
C13	1000 pF
C14	0.1μF
C15	22 mfd/6v
C16	100 pF
R1	50Ω
R2	50Ω
R7	50Ω
R8	50Ω
R9	47KΩ
R10	47KΩ
R11	47KΩ
R12	50Ω

IF Loop Filter

C6	8200 pF
C7	0.68μF
C8	0.047μF
R3	1500Ω
R4	300Ω

RF Loop Filter

C9	2700 pF
C10	0.033μF
C11	1000 pF
R5	2000Ω
R6	10KΩ

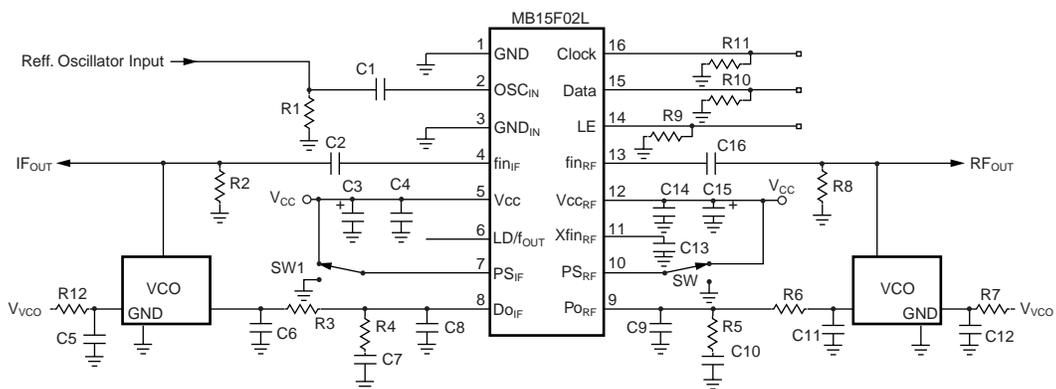


Figure 31. Application Circuit, PCS1900 Low Side Injection

Test Results at 232.5 MHz & 1775 MHz

Phase Noise Performance within the Loop = -82.3 dBc/Hz @ 232.5 MHz and -72.9 dBc/Hz @ 1775 MHz

Spurious Performance at 50 kHz from the Carrier = -88.3 dBc and at 200 kHz from the Carrier = -85 dBc

Hopping Time

1737 MHz to 1797 MHz = $498\mu\text{s}$

1797 MHz to 1737 MHz = $479\mu\text{s}$

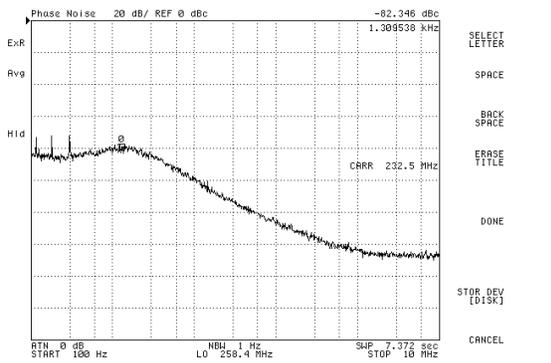


Figure 32. Phase Noise Performance C/N = -82.3 dBc/Hz

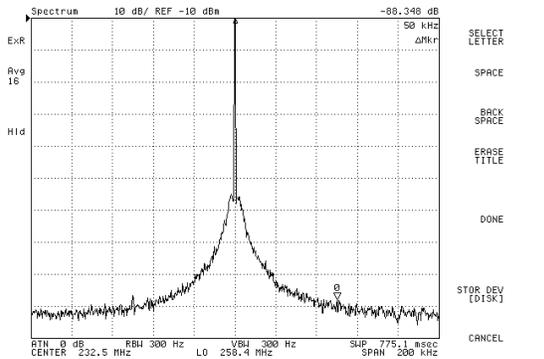


Figure 33. Spurious Performance at 232.5 MHz = -88.3 dBc

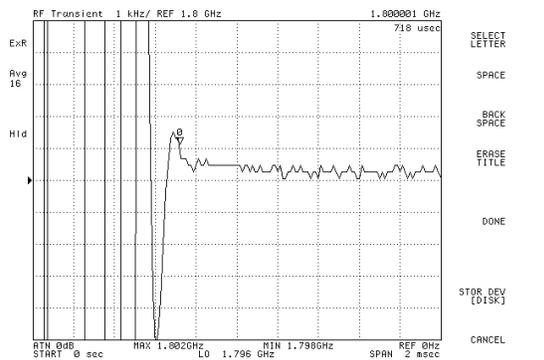


Figure 34. Hopping Time Step 1750 MHz to 1800 MHz = $718\mu\text{s}$

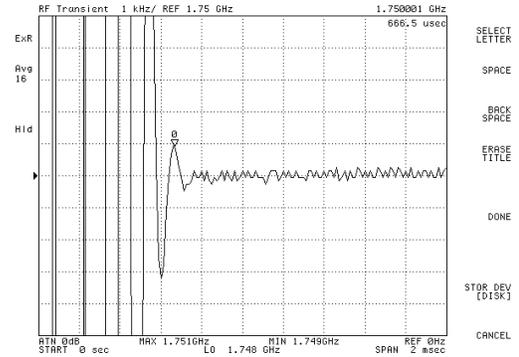


Figure 34a. Hopping Time Step 1800 MHz to 1750 MHz = $666\mu\text{s}$

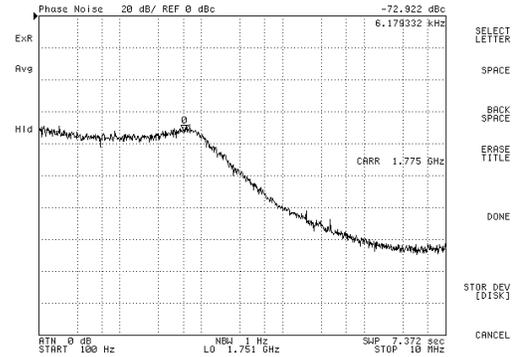


Figure 35. Phase Noise Performance C/N = -72.9 dBc/Hz

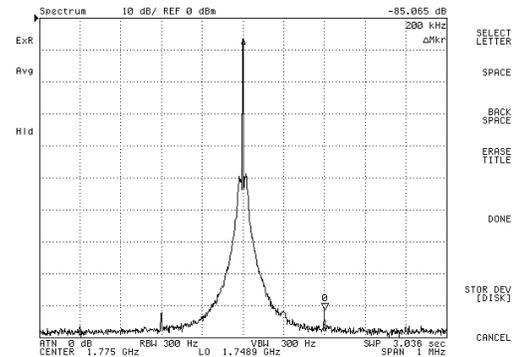


Figure 36. Spurious Performance at 1775 MHz = -85 dBc

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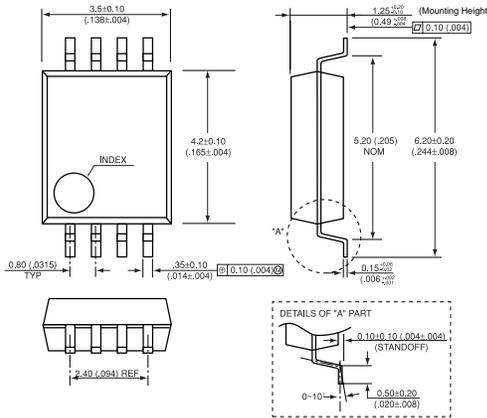


Figure 37. 8-Pin SSOP

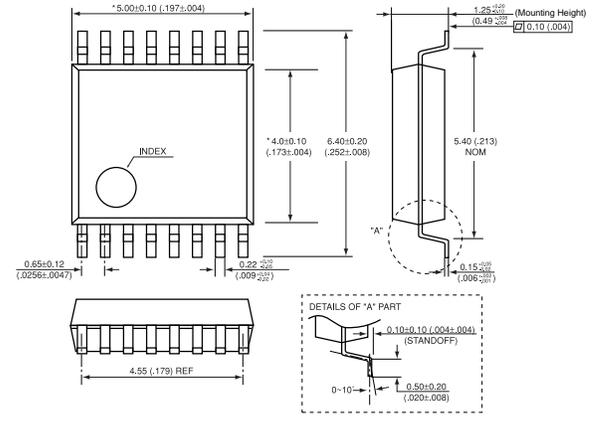


Figure 38. 16-Pin SSOP

* These dimensions do not include resin protrusion.

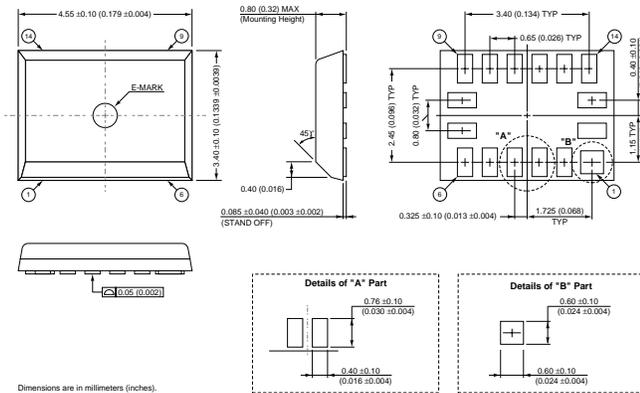


Figure 39. 16-Pin BCC (LCC-16P-M02)

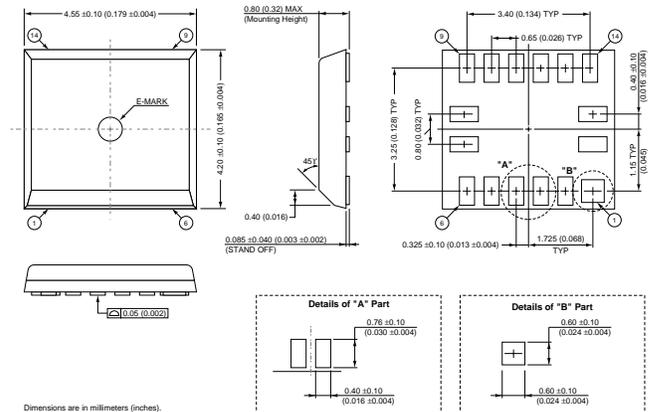


Figure 40. 16-Pin BCC (LCC-16P-M03)

Dimensions are in millimeters (inches).

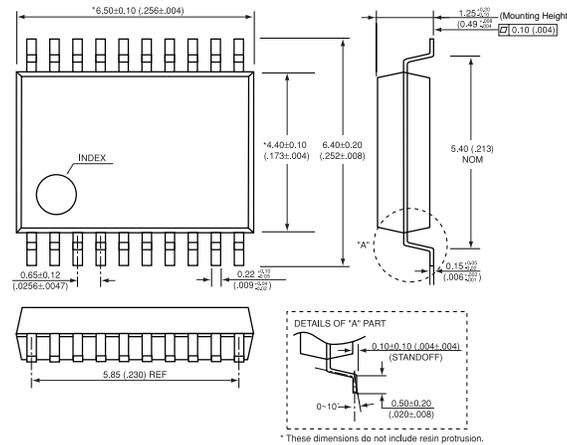


Figure 41. 20-Pin SSOP

* These dimensions do not include resin protrusion.